UNIVERSIDADE DE SÃO PAULO

ESCOLA DE ENGENHARIA DE SÃO CARLOS

DESIGNING A DIGITAL RF TRANSMISSION SYSTEM BASED ON THE NATIONAL INSTRUMENTS MYRIO PLATFORM

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SÃO CARLOS

2018

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Trabalho de Conclusão de Curso apresentado
à Escola de Engenharia de São Carlos da
Universidade de São Paulo

Curso de Engenharia Elétrica com ênfase em Eletrônica

ORIENTADOR: Prof. Dr. Evandro Luis Linhari Rodrigues

São Carlos

2018

Ficha catalográfica elaborada pela Biblioteca Prof. Dr. Sérgio Rodrigues Fontes da EESC/USP com os dados inseridos pelo(a) autor(a).

CC232d

Canton, Davi de Jesus
Designing a digital RF transmission system based on the National Instruments MyRIO platform / Davi de Jesus Canton; orientador Prof. Dr. Evandro Luis Linhari Rodrigues. São Carlos, .

Monografia (Graduação em Engenharia Elétrica com ênfase em Eletrônica) -- Escola de Engenharia de São Carlos da Universidade de São Paulo, .

1. RF transmitter. 2. BPSK. 3. myRIO. 4. ADS. 5. VHF. I. Título.

Eduardo Graziosi Silva - CRB - 8/8907

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Título: "Designing a digital RF transmission system based on the National Instruments MyRIO Platform"

Trabalho de Conclusão de Curso defendido e aprovado em 27/06/2019,

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ACKNOWLEDGEMENTS

First of all, this project was only possible because of the outstanding support of my supervisor in the UK, Prof Johannes Benedikt and my supervisor at USP, Prof. Evandro Rodrigues. In face of many harsh circumstances external to this project, I am so glad for having both of them my supervisors. Their kindness, understanding, knowledge, advice and insights go beyond expectations. I am enormously grateful. I am also eternally thankful for my family's support during hard times in pursuit of this degree and most and foremost. Above all else, I am grateful to God for His tremendous grace and mercy upon me.

ABSTRACT

In this project, we develop a wireless communication system using the National Instruments (NI) myRIO platform as well as a bespoken circuit from off-shelf electronic components. The system consists of a Binary Phase Shift Keying (BPSK) transmitter and a receiver communicating on Very High Frequency (VHF). The myRIO is responsible for the digital processing including codification and encryption of digital information while the bespoken circuits contain analogue modules responsible for the modulation, impedance matching, filtering and so on. This project aims to demonstrate great potential and capabilities of simple and accessible platforms like the NI's myRIO. They can be ideal for development and quick prototyping of more resounding systems. They can also be a great tool for proof of concepts in digital communications. Furthermore, the project develops robust hardware that completes the system. Filters, mixers and amplifiers are integrated to produce a compact yet robust proto-board solution for the BPSK transmitter and receiver. As a result, it was possible to create a reliable, encrypted and fast digital VHF point-to-point link.

Keywords: myRIO, RF transmitter, RF receiver, mixers, BPSK, ADS

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1 INTRODUCTION

Telecommunication has become one of the most important technologies in the world. Nowadays, it is just unimaginable to for the society to sustain its current operation without the current telecommunication systems. In fact, access to telecommunications is critical to the development of all aspects of a nation's economy including manufacturing, banking, education, agriculture and government. Recent World Bank studies indicate that for every US$1 invested in telecommunications infrastructure, more than US$6 is generated in economic returns by its impact on local employment and general economic growth [1]. Telecommunications were also pivotal to rapid globalization process experienced in last decades, generating further interdependence of economic and cultural activities in the world [2]. As of June 2012, over a third of the world's human population were using services from Internet [3]. As the number of users keep growing fast, so does the strain on the communication systems in current use.

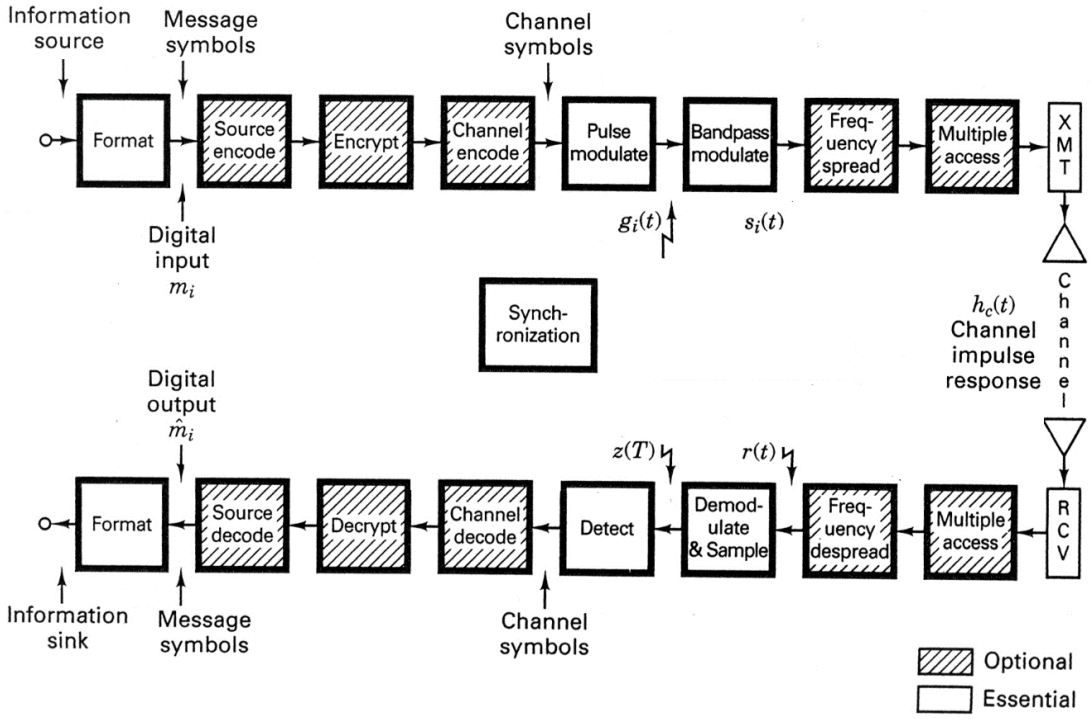
In this project, we introduce a complete telecommunication system built with the National Instruments (NI) myRIO and bespoken circuits. The report is divided into 3 units. The first section describes the theoretical and analytical background of the Digital Communication Systems (DCS). It details the main components and functionalities as well as presenting the theoretical perspective for the circuits used in the project. It starts by the description, operation and analysis of Analogue-to-Digital Converters (ADCs); encryption strategies are addressed following by Coding techniques, including Channel Coding and Line Coding. In addition, the section also explains and analyses the main forms of Modulation

The second section deals with the practical implementation of the system, including the software development, circuit design and simulations. It describes the myRIO functionalities and how it is used in this project. Then, the design of the amplifier is discussed. Next, Gilbert cells which are fundamental for modulation implementation is discussed. In the last section, the results based on test on the design will be presented and thoroughly discussed.

2 DIGITAL COMMUNICATION SYSTEMS

A digital communication system (DCS) transfers data over a communication channel, such as the air or a cable. In order to transmit information effectively, the transmitted signals need to be processed in accordance to the channel characteristics. The functional block diagram on the Figure 1 illustrates the data flow and signal-processing steps through a typical digital communication system.

Figure 1: block diagram of a general DCS



Source: [4]

The system can be divided into blocks responsible to perform several functions as follows [4]:

- *Formatting* transforms the source information into bits, thus assuring compatibility between the information and the signal processing within the system. All sources of information are analogue; therefore formatting it into a series of digital bits usually involves an Analogue-to-Digital Conversion.
- *Source encoding* attempts to compress the data from the source in order to transmit it more efficiently (basically, source encoding tries to reduce the redundancy present in the source, and represent the same information in fewer bits).

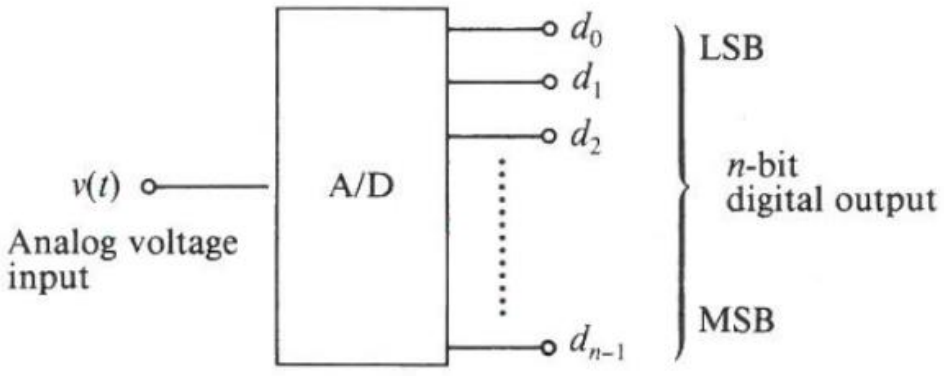
- *Encryption* encodes the information in a way that only authorized parties are able to understand it. It is usually associated with one or more numerical key that is used to codify the message.
- The performance of the system can also be improved by allocation of parity bits or convolutional codes. This class of process is called *channel coding*.
- *Modulation* is the process by which message symbols or channel symbols are converted to waveforms that are compatible with the requirements imposed by the transmission channel. Each symbol to be transmitted must first be transformed from a binary representation to a baseband waveform, this process is called *pulse modulation*; when it is applied to binary symbols, the resulting binary waveform is called a pulse-code-modulation (PCM) waveform – or line codes.
- *Frequency spreading* improves the system reliability and security by switching the waveform among many frequency channels. Generally, it uses a pseudorandom sequence known to both transmitter and receiver.

The next subsections will describe each one of them in some detail, apart from line codes and frequency spreading techniques, for they are not used in this project.

2.1 Analogue-to-Digital Conversion

Analogue-to-digital conversion is part of the process to format an analogue source into a set to a digital form. Conceptually, analogue-to-digital (AD) conversion is usually illustrated as in Figure 2 [4], where $v(t)$ is the analogue input and $d_0 \dots d_{n-1}$ is the digital output.

Figure 2: analogue to Digital Conversion general diagram.



Source: [4]

To obtain the digitized value from the analogue input, the converter (ADC) samples the input and then associates to the best digital possible value that can be represented. Those two processes are called *sampling* and *quantization*, respectively.

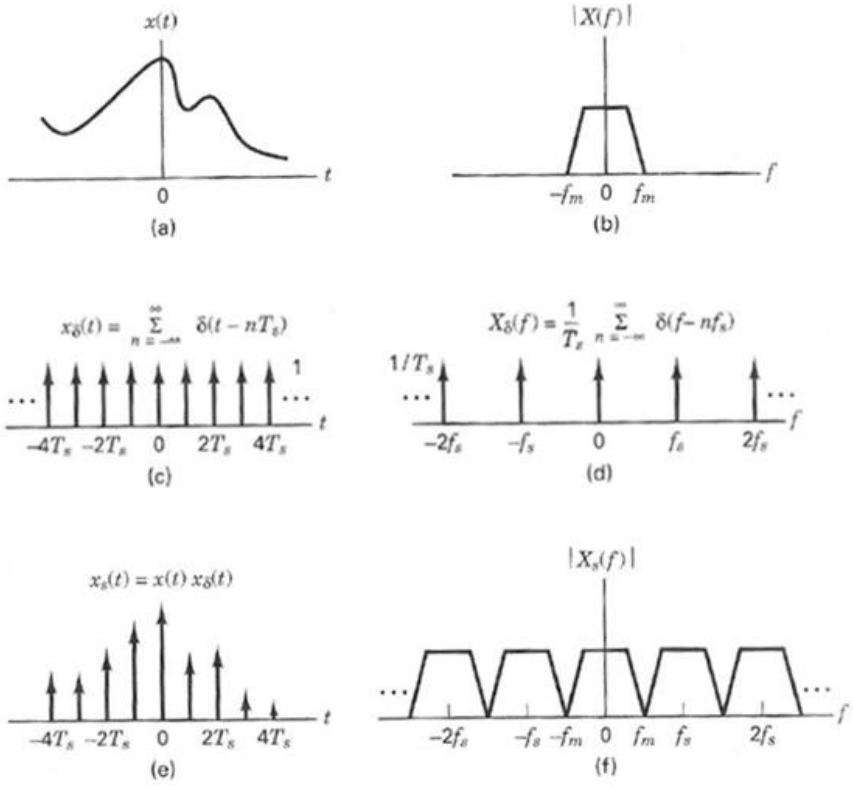
2.2 Sampling

If the input signal is acquired every T seconds (i.e. at a sampling frequency $f_s = 1/T$), then a discrete-time signal $v[n]$ can be related to the analogue signal by $v[n] = v(nT)$. The frequency in which the analogue input is sampled is very important for the design of ADCs because it defines the maximum frequency signal that can be sampled. This property is also denominated as the Nyquist-Shannon theorem.

Nyquist-Shannon sampling theorem

Assuming the analogue waveform, $x(t)$, as shown in the Figure 3(a), with a Fourier transform $X(f)$ which is zero outside the interval $(-f_m < f < f_m)$, as shown in the Firgure 3(b).

Figure 3: (a) random analogue waveform with a (b) finite frequency spectrum; (c) unit impulse train and its (d) frequency spectrum; (e) sampled signal and its (f) frequency spectrum



Source: [4]

The sampling of $x(t)$ can be viewed as the product of $x(t)$ with a periodic train of unit impulse functions $x_d(t)$ in Figure 3(c) and defined as

$$x_d(t) = \sum_{n=-\infty}^{n=\infty} \delta(t - nT_s) \tag{1}$$

Where $\delta(t)$ is the unit impulse or Dirac delta function.

Using the sifting property of the impulse function (i.e. $x(t)\delta(t - t_0) = x(t_0)\delta(t - t_0)$, it is possible to see that $x_s(t)$, the sample version of $x(t)$ shown in Figure 3(d) is given by

$$x_s(t) = x(t)x_d(t) = \sum_{n=-\infty}^{n=\infty} x(t)\delta(t - nT_s) = \sum_{n=-\infty}^{n=\infty} x(nT_s)\delta(t - nT_s) \tag{2}$$

Using the frequency convolution property of the Fourier transform, the time-domain product $x(t)x_d(t)$ can be transformed to the frequency-domain convolution $X(f) * X_d(f)$, where $X_d(f) = \frac{1}{T_s}\sum_{n=-\infty}^{n=\infty} \delta(f - nf_s)$ is the Fourier transform of the impulse train $x_d(t)$; and $f_s = 1/T_s$ is the sampling frequency.

Convolution with an impulse function simply shifts the original function as follows

$$X(f) * \delta(f - nf_s) = X(f - nf_s) \tag{3}$$

Then

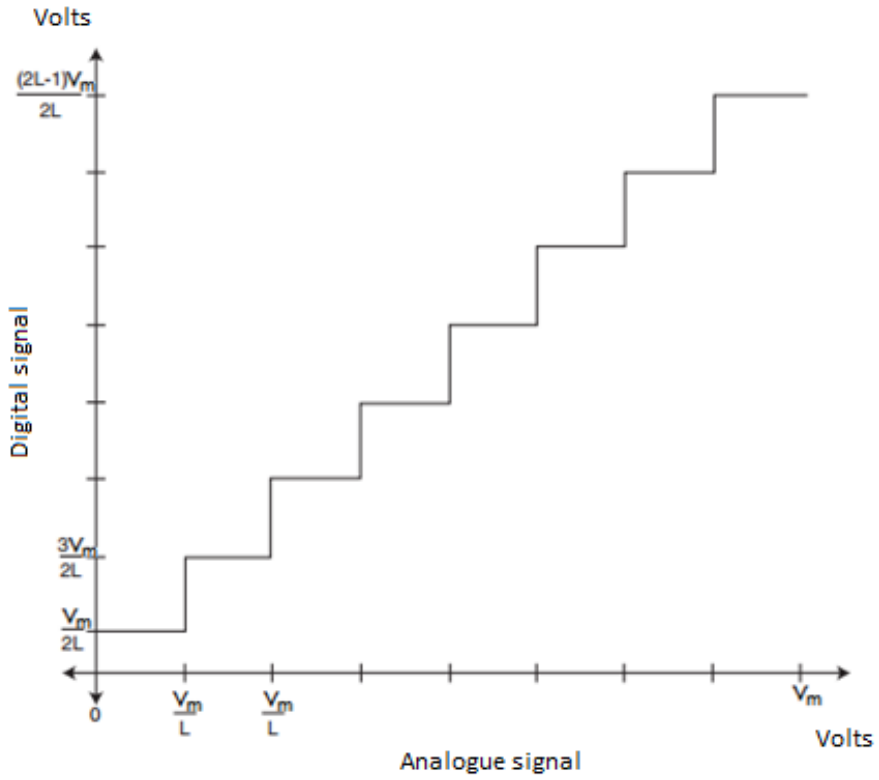
$$X_s(f) = X(f) * X_d(f) = \frac{1}{Ts} \sum_{n=-\infty}^{n=\infty} X(f - nf_s) \tag{4}$$

as shown in the Figure 3(f). So, in order to prevent that different parts of the spectrum of $x(t)$ interfere between themselves (in which case, it would be impossible to recover the original signal from the sampled values), the sampling frequency f_s must be at least twice the maximum frequency f_m present in the original signal [5][6].

2.3 Quantization

Digitally, the sampled signal can only take a discrete set of values (or levels) within a range, as shown in the Figure 4. The step between quantization levels is called quartile interval. When the quantization levels are uniformly distributed over the full range, as in the Figure 4, the quantizer is called a uniform quantizer.

Figure 4: analogue to digital codes



Source: [4]

Each sample value of the analogue input is approximated with a quantized level; the approximation will result in an error whose modulus is no larger than $L/2$. Therefore, the degradation of the signal due to quantization is limited to half a quartile interval.

A useful figure of merit for the uniform quantizer is the quantizer variance (mean-square error). If we assume that the quantization error, e, is uniformly distributed over a single quantile interval q-wide (i.e. the analogue signal input takes on all values with equal probability), the quantizer error variance is found to be

$$\sigma^2 = \int_{-q/2}^{+q/2} e^2 p(e) de = \int_{-q/2}^{+q/2} e^2 \frac{1}{q} p(e) de = \frac{q^2}{12} \quad (5)$$

where $p(e) = 1/q$ is the probability density function of the quantization error. The variance, σ^2, corresponds to the average quantizaion noise power. The peak power of the analog signal (normalized to 1Ω) can be expressed as

$$V_p^2 = \left(\frac{V_{pp}}{2}\right)^2 = \left[\frac{q(L-1)}{2}\right] \approx \left(\frac{Lq}{2}\right)^2 = \frac{L^2 q^2}{4} \quad (6)$$

where *L* is the number of quatization levels. Therefore, the ration of peak singal power to average quantization noise power (SNRQ) is

$$\left(\frac{S}{N}\right)_q = \frac{L^2 q^2/4}{q^2/12} = 3L^2 \quad (7)$$

Therefore, fewer digital levels implies higher quantization noise. Modern AD Converters are able to minimize this noise to almost insignificant values when compered the thermal noise, which is inherent in the system [7][8].

2.4 Encryption

The two primary reasons for using cryptosystems in communications are privacy (to prevent unauthorized person from extracting information from the channel) and authentication (to prevent unauthorized person from inserting information into the channel). The general concept of cryptography involves a message M being encrypted by the use of an invertible transformation $E_K(M)$ that produces a cyphertext $C = E_K(M)$, which is transmitted over an insecure or public channel [4]. When an authorized recover obtains C, he decrypts it with the inverse transformation $D_K = E_K^{-1}[E_K(M)] = M$. The parameter K refers to the key, which dictates the encryption transform E_K.

RSA Cryptography

In the RSA Cryptography the messages are first represented as integers in the range $(0, n-1)$. Each user chooses its own value of n and another pair of positive integers e and d. The number pair (n, e) is the user encryption key, which is public. The decryption key consists of the pair (n, d), which d is kept secret.

Encryption of a message M and decryption of a cyphertext C are defined as follows

$$C = E(M) = (M)^e mod\ n \quad (8)$$

$$M = D(C) = (C)^d mod\ n \quad (9)$$

In RSA scheme, n is obtained by selecting two large prime numbers p and q and multiplying them together:

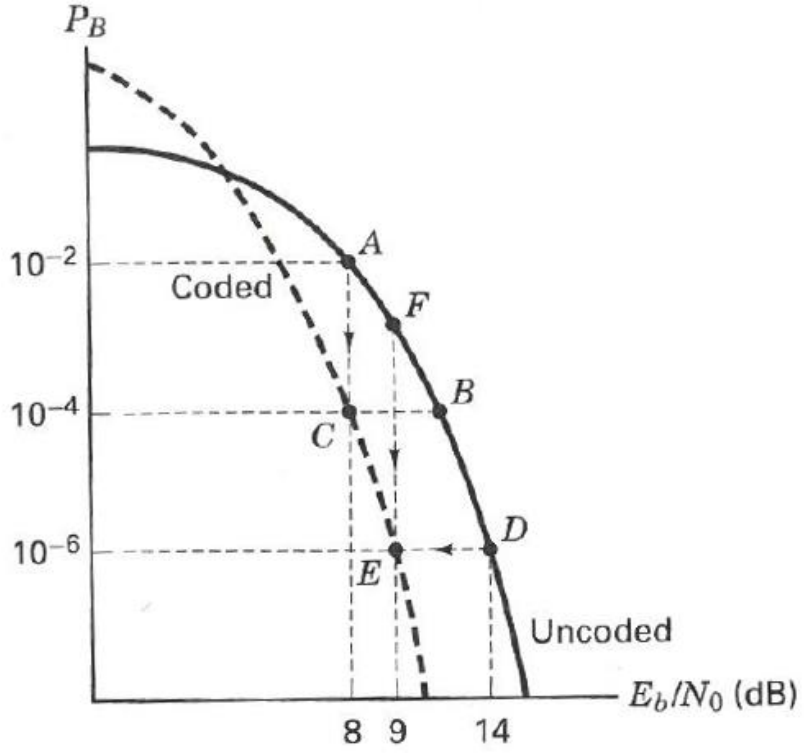
$$n = pq \quad (10)$$

Although n is made public, the numbers p and q are kept hidden, due to the great difficult in factoring n [4].

2. 5 Channel Coding

Channel coding methods are very effective on the reduction of errors in the received signal [4]. Figure 5 shows the comparison between the bit-error from a raw signal and a coded signal. For high signal to noise ratios, coding presents a definitive advantage.

Figure 5: bit-error performance versus the Signal to Noise Ratio (SNR) for coded and raw data, P_B is the error probability, E_b is the signal energy and N_0 is the noise energy.



Source: [4]

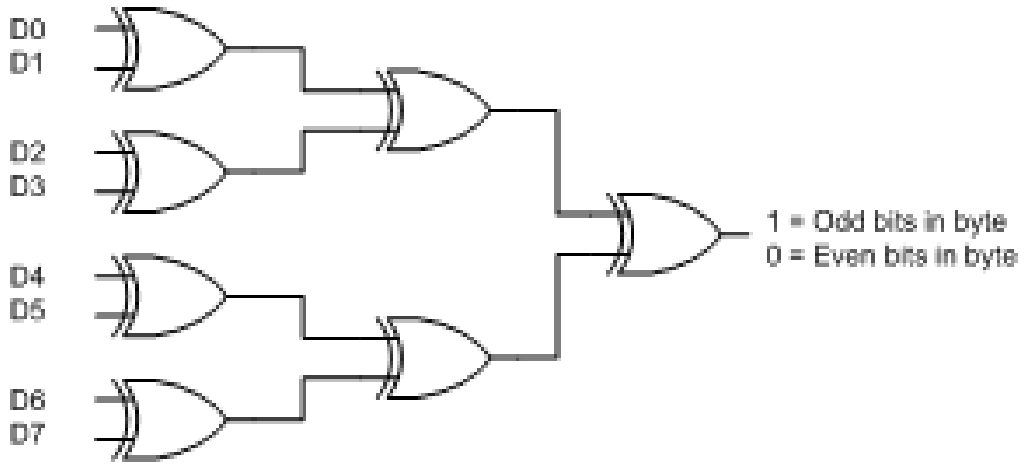
The various coding methods are achieved by interweaving additional binary digits into the transmission. So, when decoding in the receiving end, it is possible to check for errors that may have occurred in the transmission. In many cases, it is also possible to repair the errors.

Single Parity Check

Parity-check codes use linear sums of the information bits, called parity symbols, for error detection and correction. A single-parity check – the simplest of the channel coding methods - is constructed by adding a single-parity bit to a block of data bits. The parity bit is set as such the summation of all bits in the codeword yields to an even (or odd) result.

Usually, this summation operation is performed using exclusive-or logic (modulo-2 arithmetic), as shown in the Figure 6.

Figure 6: 8-bit hardware-based parity generator



Source: [4]

At the receiving terminal, the decoding procedure consists of testing that the modulo-2 sum of the codeword bits yields to a zero result (even parity). If the result is different, the codeword is known to contain errors; however, the single parity check is not able to correct an error - only detect it [4].

Rectangular Code – 2D Parity Check

The rectangular code can be thought of as a parallel structure, depicted in Figure 7, in which the data is arranged as a rectangle, then a horizontal parity check is append to each row and a vertical parity check is append to each column.

Figure 7: example of an 8-bit 2D parity check

0110100	1
1011010	0
0010110	1
1110101	1
1001011	0
1000110	1

Any bit error would case a parity check failure in one of the array columns as well as one of its rows. Therefore, the rectangular code is able to correct any single error.

2.6 Modulation and Demodulation

Modulation converts information from a baseband signal into a high-frequency signal. Generally it modifies one or more properties of a carrier waveform - such as amplitude, frequency or phase – according to a modulating baseband signal.

Amplitude modulation

The amplitude of the carrier signal, $V_c(t)$, is modulated by a signal $V_m(t)$. If carrier $v_c(t) = V_c\cos(w_c t)$ is multiplied by the modulating signal $v_m(t) = V_m\cos(w_m t)$, then the output is

$$V(t) = \frac{1}{2}kV_mV_c\{\cos(w_m + w_c)t + \cos(w_m - w_c)t\} \quad (11)$$

Where k is the constant of the multiplier.

The output of the modulator therefore contains two components, one above and one bellow the carrier. Each one is separated from the carrier by an amount w_m $(-2\pi f_m)$ so that the bandwidth occupied by the signals is $\pm f_m$. In this case, there is no component at f_c, i.e. this is a double-sideband suppressed-carrier (DSBSC) signal [9].

Phase Shift Keying

The general analytic expression for PSK is [4]

$$S_i(t) = \sqrt{\frac{2E}{T}}\cos\big(w_0 t + F_i(t)\big) \tag{12}$$

Where the phase term $F_i(t)$ will have M discrete values, typically given by

$$F_i(t) = \frac{2\pi}{M}, \quad i = 1,2,..,M \tag{13}$$

BPSK

In Binary Phase Shift Keying (BPSK), the phase of the carrier signal is switched between two values acceding to two possible signals m_1 and m_2 corresponding to binary 1 and 0, respectively. Normally, the two phases are separated by 180^o. If the sinusoidal carrier v_c has an energy per bit $E_b = \frac{1}{2}A_c^2 T_b$, then the transmitted BPSK signal is either

$$s_{BPSK}(t) = \sqrt{\frac{2E_b}{T_b}}\cos(\omega_c t + \theta_c), \quad 0 \le t \le T_b \tag{14}$$

Or

$$s_{BPSK}(t) = -\sqrt{\frac{2E_b}{T_b}}\cos(\omega_c t + \theta_c), \quad 0 \le t \le T_b \tag{15}$$

The BPSK signal can also be expressed as

$$s_{BPSK}(t) = m(t)\sqrt{\frac{2E_b}{T_b}}\cos(\omega_c t + \theta_c) \tag{16}$$

Where $m(t)$ is a non-return to zero (NRZ) signal, which is either $+1$ or -1.

BPSK Receiver:

If no multipath interferences are induced by the channel, the received BPSK signal is given by

$$s_{BPSK}(t) = m(t)\sqrt{\frac{2E_b}{T_b}}\cos(\omega_c t + \theta_c + \theta_{ch}) \tag{17}$$

Where θ_{ch} is the phase shift corresponding to the time delay in the channel. BPSK uses coherent or synchronous demodulation, which requires that information about the phase and frequency of the carrier be available at the receiver. If a pilot carrier signal is transmitted

along with the BPSK signal, then the carrier phase and frequency may be recovered at the receiver using a phase looked loop (PLL). If no pilot carrier is transmitted, a Costas loop may be used to synthesize the carrier phase and frequency from the received BPSK signal.

QPSK

In QPSK, the data bits to be modulated are grouped into symbols, each containing two bits, and each symbol can take on one of four possible values: 00, 01, 10, or 11. During each symbol interval, the modulator shifts the carrier to one of four possible phases corresponding to the four possible values of the input symbol. In the ideal case, the phases are each 90 degrees apart.

Practical QPSK modulators are often implemented using the trigonometric identity

$$I \cos w_c t + Q \cos(w_c t + \theta) = R \cos(w_c t + \theta) \quad (18)$$

Where $R = \sqrt{(I^2 + Q^2}$ and $\theta = \tan^{-1} Q/I$.

2.7 Amplifiers

The portion of the wave cycle the device spends in its active region (i.e. behaves as a controlled-current source) is the *conduction angle* and it is denoted by $2\theta_c$.

Classification [10]

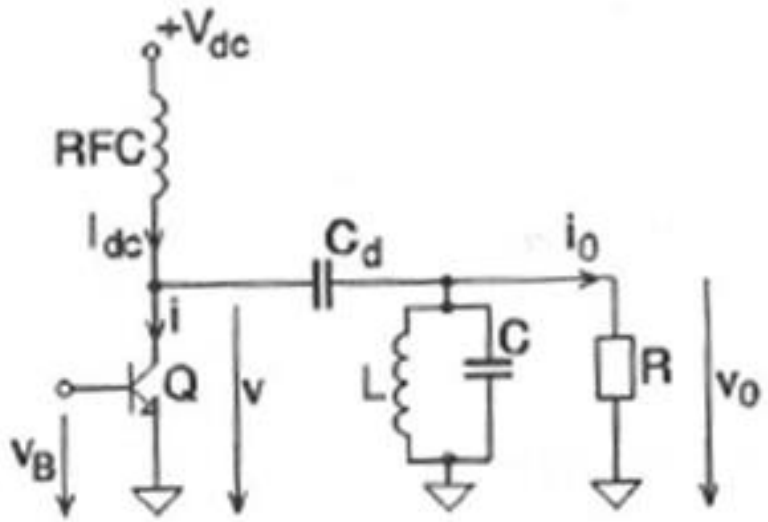
- Class A amplifiers, if $2\theta_c = 360^o$. The active device is in its active region during the entire RF cycle. For Class A operation, the quiescent point (Q) must be selected to keep the transistor in its active region during the entire RF cycle, thus assuring a 360 degree conduction angle.
- Class AB amplifiers, if $180^o < 2\theta_c < 360^o$
- Class B amplifiers if $2\theta_c = 180^o$.
- Class C amplifiers, if $2\theta_c < 180^o$.

Generally, all these amplifiers use the same basic collector circuit topology of Figure 8. This is a single-ended circuit, in which the transistor operates in the common-emitter configuration; however, common-base configurations are also possible. The collector circuit includes an RF choke (RFC) that provides a constant (DC) input current, I_{dc}, a DC-blocking

capacitor, C_d, the load resistor R and a parallel resonant LC circuit tuned to the operation frequency.

For Class A operation, the quiescent point (Q) must be selected to keep the transistor in its active region during the entire RF cycle, thus assuring a 360 degree conduction angle.

Figure 8: basic circuit topology for common emitter BJT amplifier



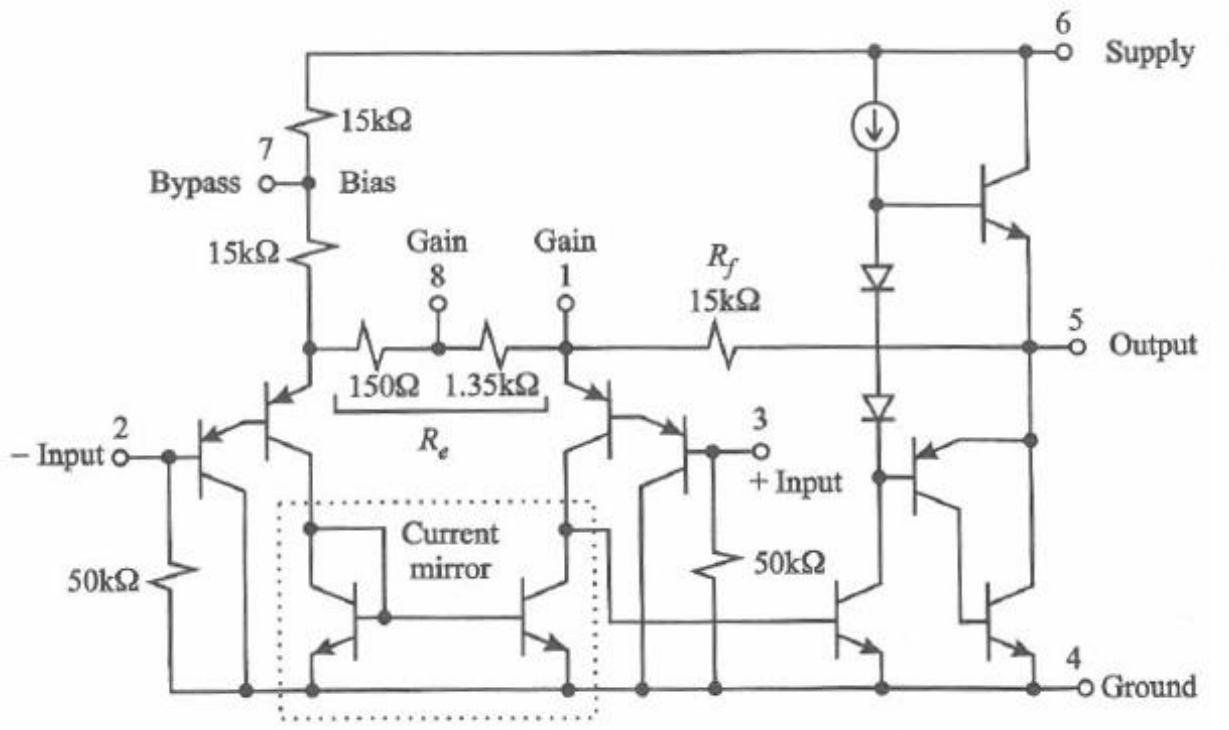
Source: [10]

Differential Amplifiers

For a differential amplifier with inputs v_1 and v_2, we define the *differential-mode input* voltage as $v_d \equiv v_1 - v_2$ and the *common-mode input* voltage as $v_{cm} = \frac{v_1+v_2}{2}$.

The Figure 9 shows the schematic for the LM386N-1. There are three stages of amplification. The input is a differential amplifier. Each input has a pair of stacked pnp transistors, which give a current gain of β^2. The differential amplifier is followed by a common-emitter stage. The output is a Class-B emitter follower. The feedback resistance R_f and the emitter resistance R_e determine the gain of the amplifier.

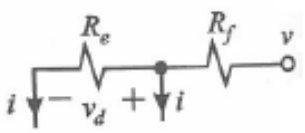
Figure 9: LM386N-1 schematic



Source: Texas Instruments – LM386 Datasheet

The collector loads for the differential amplifier is a current mirror, which forces the collector currents to be the same. So we can simplify the Amplifier as in the Figure 10. Here v is the AC output voltage. The currents labeled i at each end of the emitter resistance R_e are forced to be equal by the current mirror. The voltage across $R_e$is the differential voltage v_d.

Figure 10: simplified schematic of the LM386N-1



Source: [10]

Therefore, the current that flows through the feedback resistor R_f is approximately $2i$. The current that flows in the two $15k\Omega$ bias resistors is negligible because these have a much higher impedance than the pnp emitters, which are basically forward-biased diodes. Thus,

$$2i \approx \frac{v}{R_f} \tag{19}$$

assuming that the voltage v is much higher than the voltage v_d due to the gain of the amplifier. Also,

$$i = \frac{v_d}{R_e} \tag{20}$$

Therefore, the voltage gain is

$$G_v = \frac{v}{v_d} = \frac{2R_f}{R_e} \tag{21}$$

An advantage of this circuit is that the voltage gain only depends on the feedback and emitter resistances, not on the β of transistors, which can be quite variable. [11]

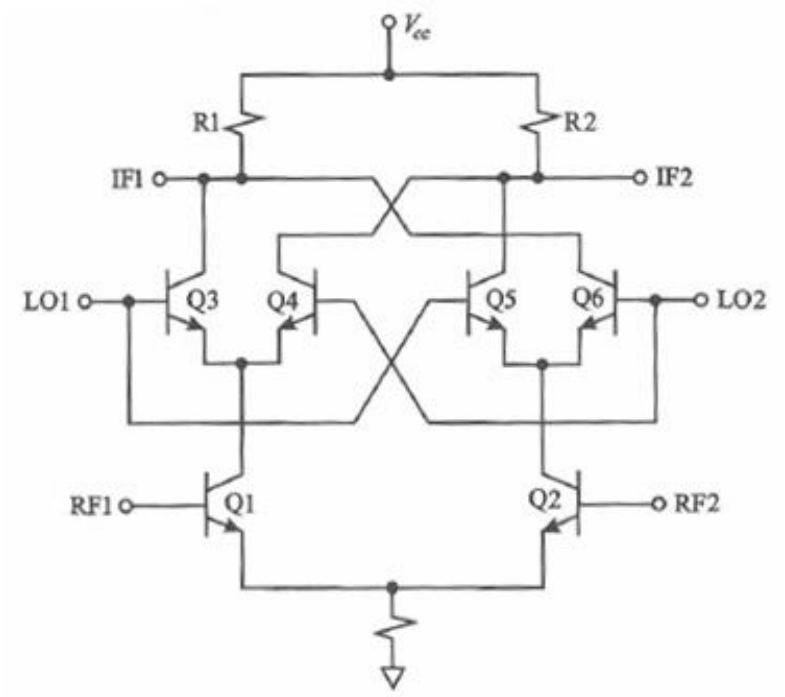
Mixers

Mixers shift signals from one frequency to another.

Gilbert Cell

It is simple mixer circuit [11] composed of a cross-coupled differential amplifier, as shown in the Figure 11, where the gain is controlled by modulating the emitter bias current.

Figure 11: Gilbert Cell, basic schematic



Source: [11]

On the bottom, we can see a pair differential amplifier, with RF1 and RF2 signal inputs. However, inserted between the collectors and the collector resistors are four cross-

coupled transistors. These are driven by the local oscillators. To understand the effect of the local oscillator assume that the voltage of at LO1 is large, so that Q3 and Q5 turn on. This connects Q1 to R1 and Q2 to R2, and we have a normal differential amplifier. Now consider what happens if the voltage at LO2 is large, so that Q4 and Q6 are turned on. This connects Q1 to R2 and Q2 to R2. We have a differential amplifier again, but the outputs are interchanged. This changes the sign of the outputs. The effect is that the output is alternately multiplied by +1 and -1 depending on the sign of the local oscillator. Assuming RF2 grounded and the voltage at RF1 as $V_1(t)$ given by

$$V_1(t) = V_1 \cos(w_1 t) \tag{22}$$

The Fourier components for the LO is

$$V_{lo}(t) = \frac{4}{\pi}\left(\cos w_{lo}t - \frac{1}{3}\cos 3w_{lo}t + \frac{1}{5}\cos 5w_{lo}t + \cdots\right) \tag{23}$$

So

$$V(t) = V_1(t)V_{lo}(t) \tag{24}$$

Expanding that

$$V(t) = \frac{2V_1}{\pi}\left(\begin{array}{c}\cos(w_{lo}t - w_1 t) - \frac{1}{3}\cos(3w_{lo}t - w_1 t) \\ + \frac{1}{5}\cos(5w_{lo}t - w_1 t) + \cdots\end{array}\right) \tag{25}$$

From these sums, we can identify the sum and the difference frequency terms V+ and V-:

$$V_+(t) = \frac{2V_1}{\pi}\cos(w_+ t) \tag{26}$$

$$V_-(t) = \frac{2V_1}{\pi}\cos(w_- t) \tag{27}$$

Where $w_+ = w_{lo} + w_1$ and $w_- = |w_{lo} - w_1|$.

2.8 Phase-Looked Loop (PLL)

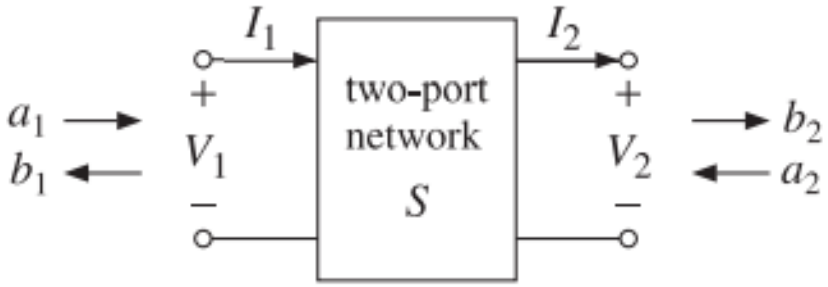
The phase-looked loop (PLL) is an analogue circuit, which uses a negative feedback control loop to produce both an oscillator output frequency synchronized with an input signal frequency, and an output voltage proportional to input signal frequency changes [12].

2.9 Filters

Scattering Parameters

A linear two-port network as shown in the Figure 12 can be characterized by a number of different circuit parameters, such as its transfer (ABCD) matrix, impedance matrix or scattering matrix.

Figure 12: two-port network



Source: [10]

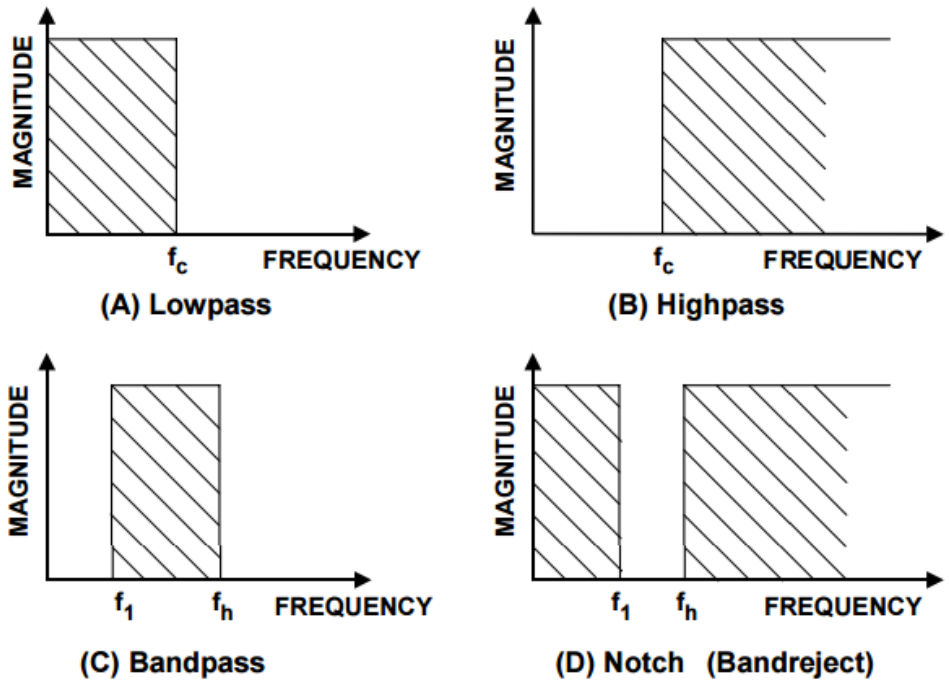
The *scattering matrix* relates the outgoing waves b_1, b_2 to the incoming waves a_1, a_2 that are incident in the two ports, so that $[b_1 \quad b_2]^T = S[a_1 \quad a_2]^T$ where

$$S = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \tag{28}$$

The matrix elements S_{11},S_{12},S_{21},S_{22} are referred as the scattering parameters or S-parameters [13]. The physical meaning of S_{11} is the input reflection coefficient, S_{21} is the forward transmission gain, S_{12} is the reverse transmission gain and S_{22} is the output reflection coefficient.

The ideal filter [14] will have an amplitude response that is unity (or at a fixed gain) for the frequencies of interest (called the pass band) and zero everywhere else (called the stop band). The frequency at which the response changes from passband to stopband is referred to as the cut-off frequency.

Figure 13: ideal filter response; (a) low-pass filter, (b) high-pass filter, (c) band-pass filter, (d) band-reject filter



Source: [4]

If a high-pass filter and a low-pass filter are cascaded, a band pass filter is created. The band pass filter passes a band of frequencies between a lower cut-off frequency, f_1, and an upper cut-off frequency, f_h. Frequencies below f_1 and above f_h are in the stop band. An idealized band pass filter is shown in Figure 13.

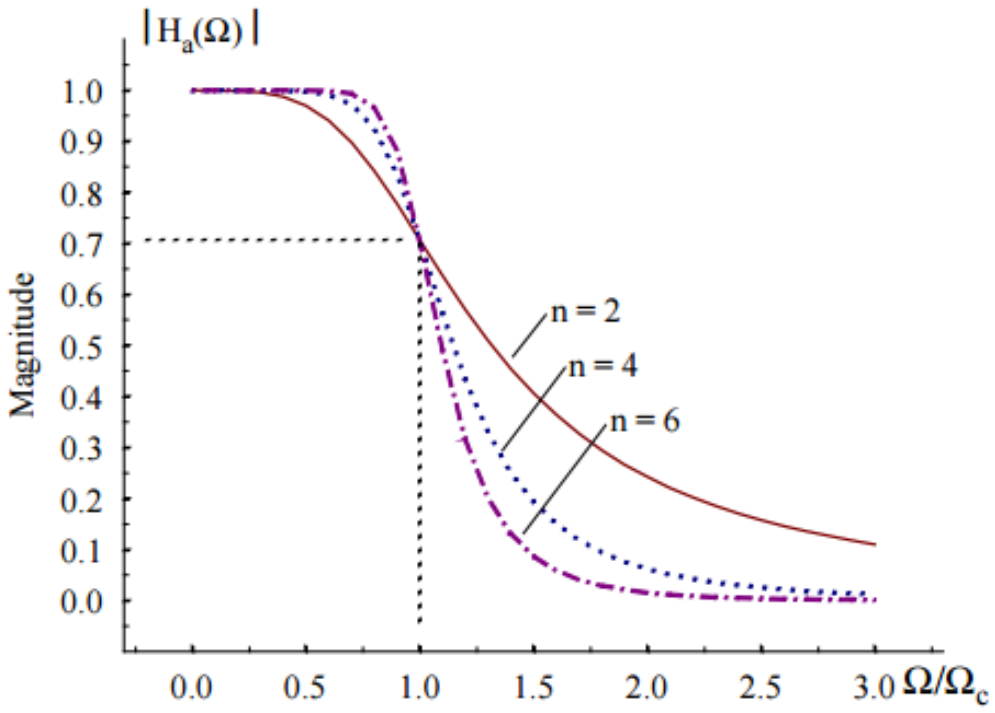
Low Pass Filters

The squared magnitude function for an n-order Butterworth low-pass filter is

$$|H_a(j\Omega)|^2 = H_a(j\Omega)H_a^*(j\Omega) = \frac{1}{1+\left(\frac{j\Omega}{j\Omega_c}\right)^{2n}} \tag{29}$$

Where constant Ω_c is the 3dB cut-off frequency. Magnitude $|H_a(j\Omega)|$ is depicted by Figure 14.

Figure 14: magnitude for a Butterworth filter of order 2, 4 and 6.



Source: [10]

2.10 Antennas and Propagation Models

Free Space Propagation Model

The free space propagation model [15] is used to predict received signal strength when the transmitter and receiver have a clear, unobstructed line-of-sight path between them. The free space power received be a receiver antenna which is separated from a radiating transmitter antenna by a distance d, is given by the Friis free space equation

$$P_r = \frac{P_t G_t G_r \lambda^2}{(4\pi)^2 d^2 L} \tag{30}$$

Where P_t is the transmitted power, $P_r(d)$ is the received power which is a function of the separation, d, between the transmitter and the receiver, G_t is the transmitter antenna gain, G_r is the receiver antenna gain, L is the system loss factor not related to propagation, and λ is the wavelength in meters.

The Friis free space equation shows that the received power falls off as the square of the transmitter-receiver distance. This implies that the received power decays with distance at the rate of $20dB/decade$.

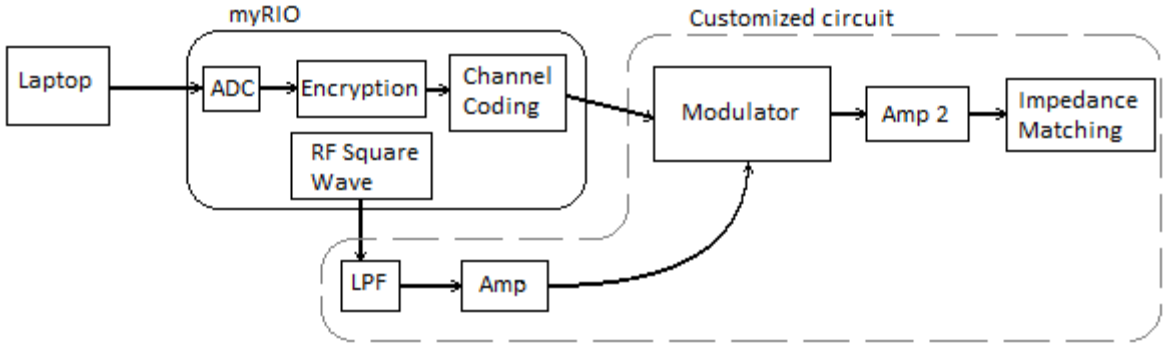
The *path loss* is the difference between the effective transmitted power and the received power (in dB). The path loss for the free space model when the antenna gains are included is given by

$$PL(dB) = 10\log\frac{P_t}{P_r} = -10\log\left[\frac{\lambda^2}{(4\pi)^2 d^2}\right] \tag{31}$$

3 IMPLEMENTATION

This project implements the concepts addressed in the previous sections. The complete Communication System is created, based on the National Instrument (NI) myRIO platform working together with a bespoken analogue circuit responsible for transmission and reception of signal.

Figure 15: transmitter diagram



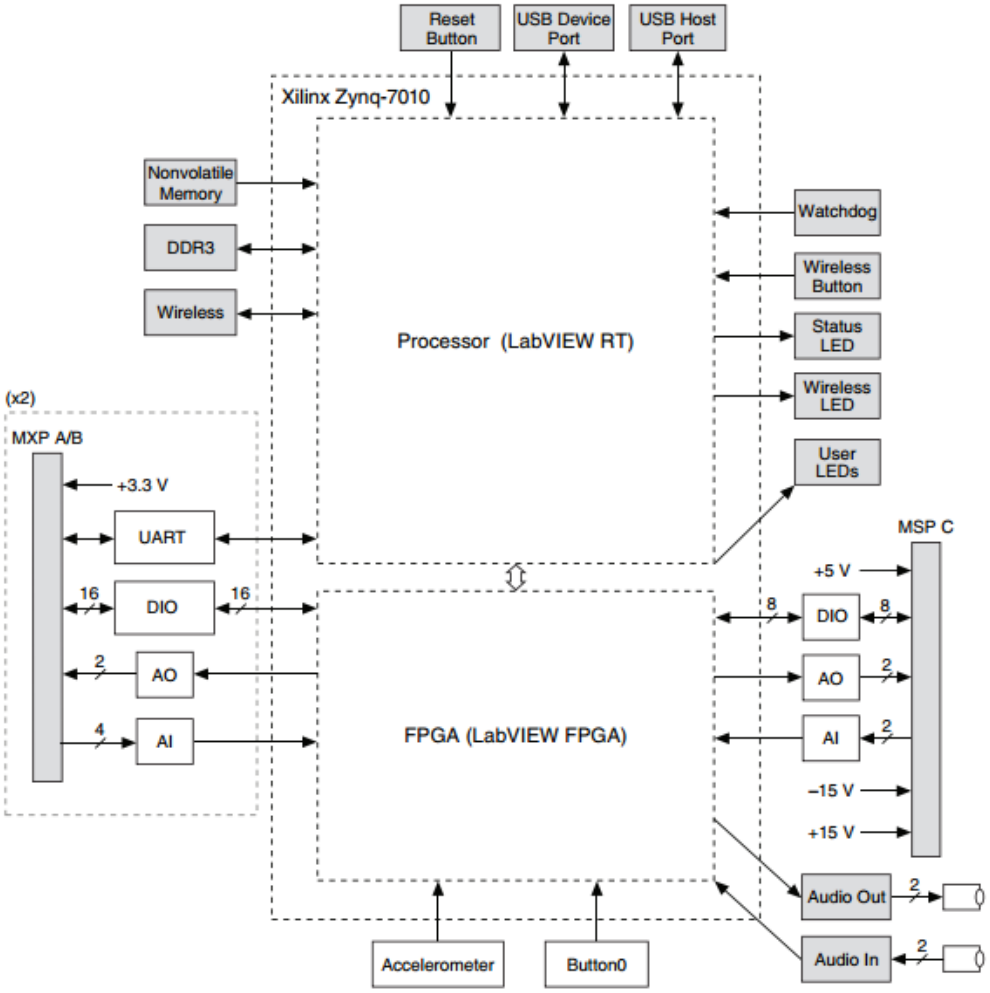
The transmission system works as follows: an audio output (from a laptop, in this case) is fed to one of the audio inputs in the myRIO, which contains an embedded Analogue to Digital Converter (ADC) that transform the analogue signal into binary that in double integer representation. This sampled value, both from left and right channels, is encrypted using RSA cryptography, then it is coded (i.e. a parity bit is added) in order to reduce the possibilities of errors on the reception end. The myRIO outputs this data as a digital wave stream to the customized board as well as a digital waveform at Very High Frequency (VHF) - in the tests the frequency used was 88MHz – from which an analogue carrier wave is extracted using a low-pass filter and an amplifier. The BPSK modulator module switches the carrier wave polarity according to data stream. The RF signal is then amplified and matched to an external antenna.

The following subsections present the construction details and design of those building blocks.

3.1 LabView circuits for myRIO

The National Instruments myRIO is portable reconfigurable I/O (RIO) platform. It contains an embedded dual-core 667 MHz Xilinx processor as well as an embedded FPGA. Figure 16 shows its main modules.

Figure 16: myRIO block diagram



Source: NI myRIO-1900 User Guide and Specifications

The fixed processor implements the ARMv7 instruction set architecture (ISA) and includes a fixed set of peripherals. The ARM Cortex-A9 on myRIO is preconfigured at the factory with a distribution of Linux with real-time extensions. The NI LabVIEW is used to compile, download, execute and debug Structured Dataflow applications on myRIO.

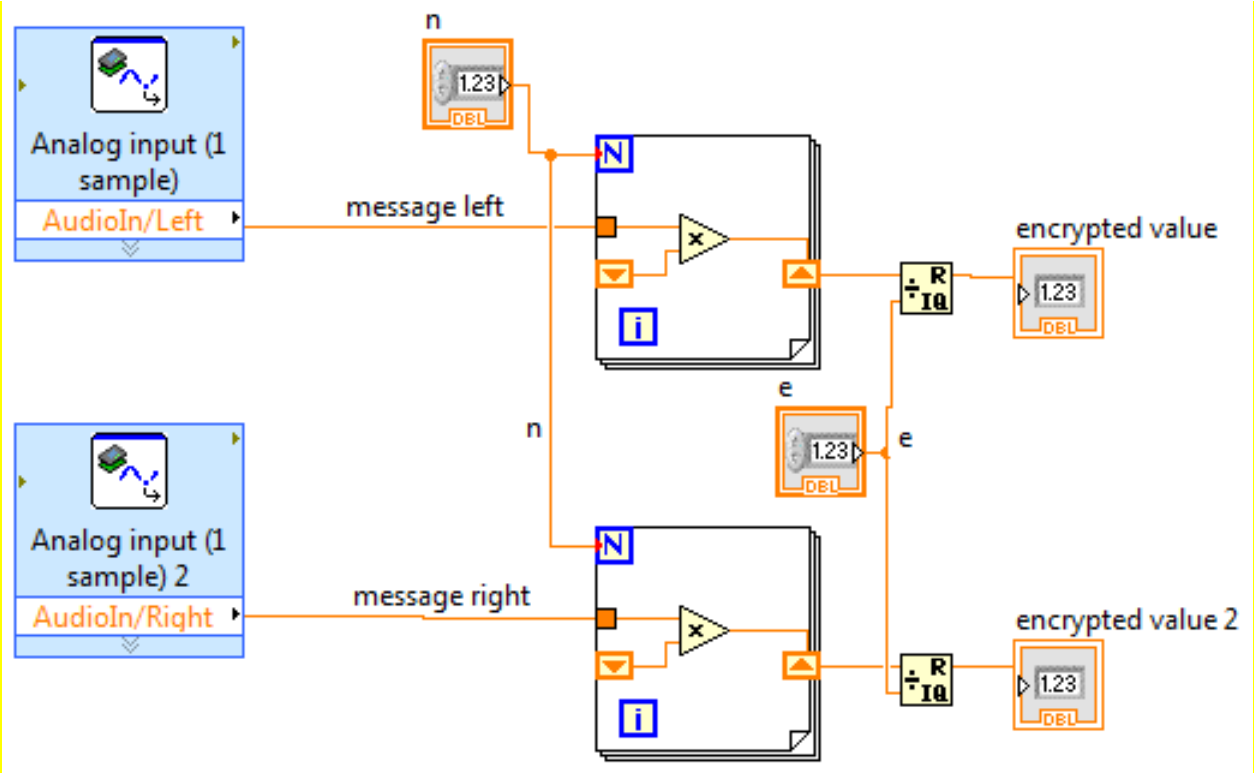
Analogue to Digital Conversion

The myRIO 1900 contains a 12-bit Analogue to Digital Converter, which does not require any programming. In real-time, the hardware automatically converts the analogue audio input into a double int number.

Encryption

The digital double int inputs are cryptographed in order to increase security of information in the system. The simplified RSA algorithm is use, as shown on the LabVIEW diagram in the Figure 17. It basically calculates the value for the cyphertext given by: $(message)^n mod(e)$.

Figure 17: encryption LabVIEW diagram



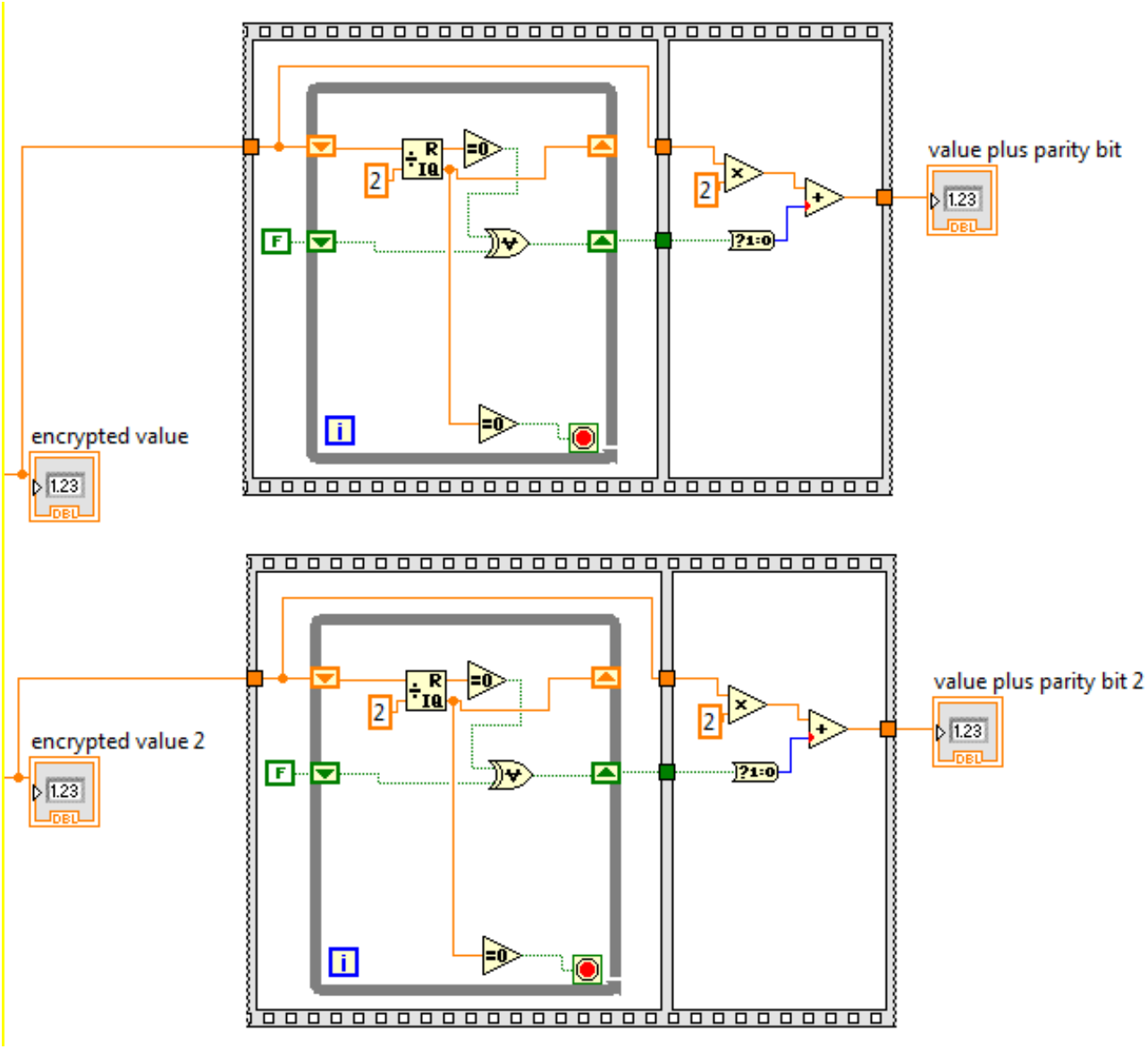
The values *n* and *e* are the public key of the system. They are obtained from two large prime numbers *p* and *q* implemented in an auxiliary C program.

Channel Encoding

This module inserts a parity digit in the end of the data, as shown in the Figure 18. The while block returns a Boolean variable which is true if the number of bits in the word with value 1 is odd and returns false, otherwise. This information is used to insert a new bit by the

end of the word so that the number of bits with value 1 is always even. This approach enables to detect any single-bit error; however, it does not provided a way to correct it.

Figure 18: channel encoding LabVIEW diagram

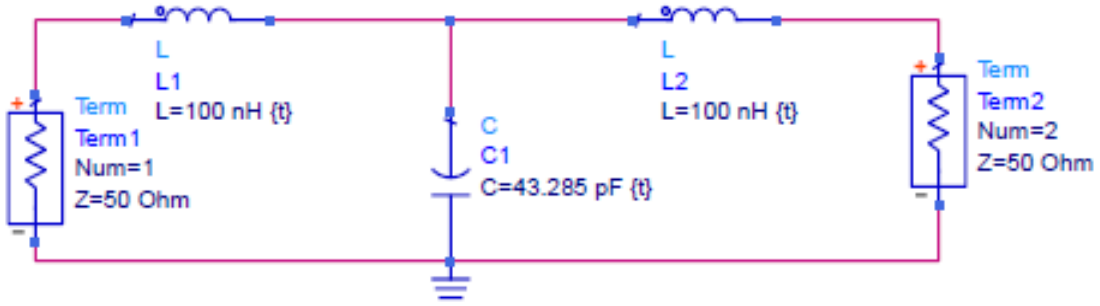


3.2 Filters

Carrier Extraction

In the transmitter, a low-pass filter is used to obtain the carrier wave from the digital waveform provided by the myRIO, as shown in the Figure 19. The filter attenuates all frequencies above the fundamental harmonic, at $f_c = 88\,MHz$. This is a Butterworth filter. The value of the capacitances, inductances and resistors were then adjusted in the simulation.

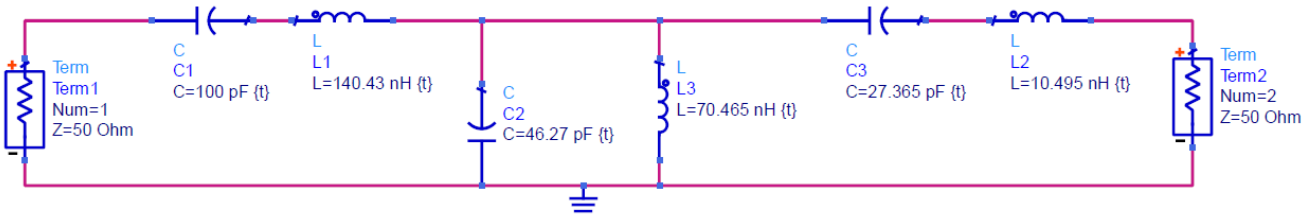
Figure 19: low-pass filter for carrier extraction



Band Pass Filters

The modulation process might generate undesired harmonics into the system in addiction to impurities from thermal and environmental noise. Therefore a Band Pass Filter (BPF) is necessary to make sure that only the uncorrupted modulated signal is amplified. Figure 20 shows a Butterworth BPF design. The values were tuned through an ADS simulation of the filter.

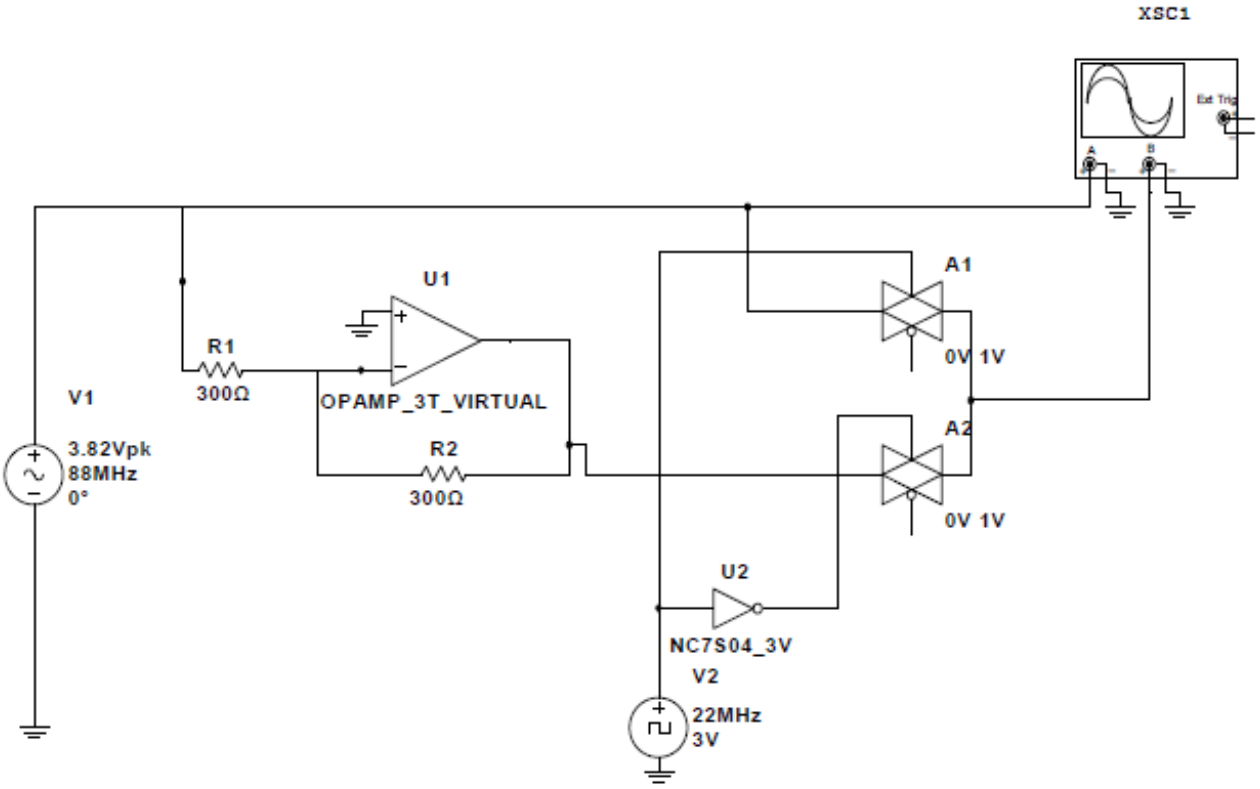
Figure 20: band-pass filter centred at 88MHz



3.3 Modulation

Since we use BPSK in this project, the circuit to implement the modulation scheme is fairly simple, as shown in the Figure 21. The design consists of an unit-gain inverting amplifier, which splits the carrier wave into two complementary RF signals. Only one of them is transmitted at a time. This process is digitally controlled by two switches connected to the data stream, modulating therefore the carrier wave.

Figure 21: virtual circuit of the BPSK modulation using an inverting amplifier and digitally controlled switches

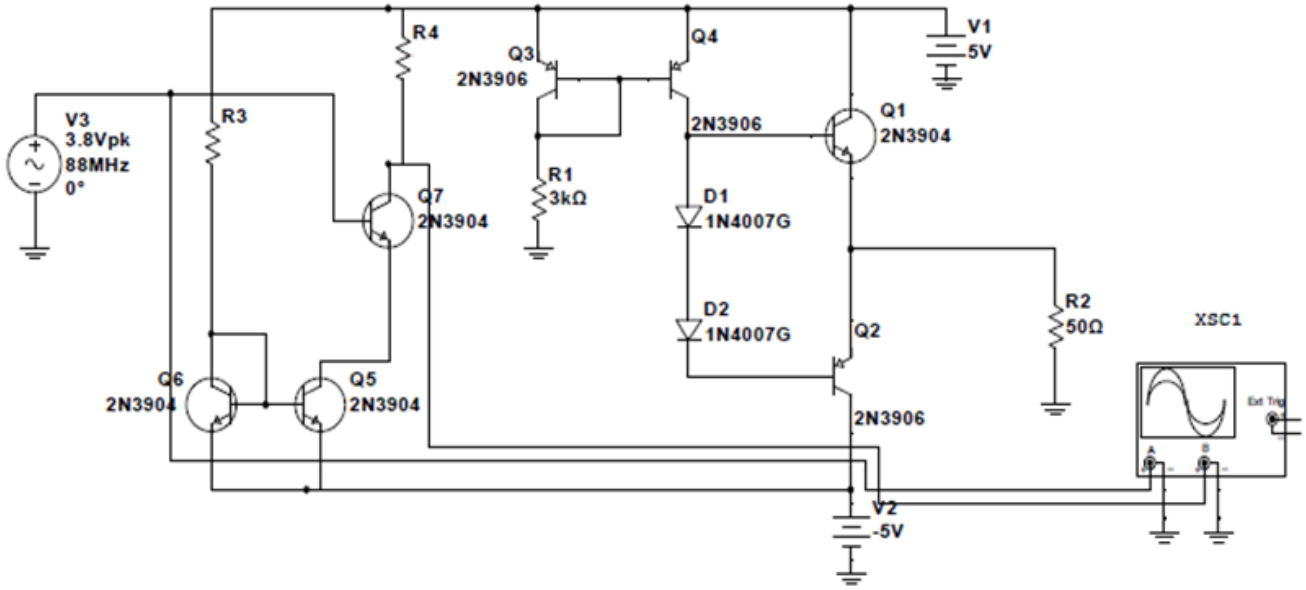


In the hardware implementation, a CWB201 fast Quad Switch is used.

3.4 Power Amplification

After being modulated, the signal is then amplified to satisfy the transmission requirements. The idea is that the power transmitted must be as such that it is possible to recover completely the information transmitted using a receiver located in a different room within 200m range. The circuit at the Figure 22 shows the 2-stage power amplifier circuit designed.

Figure 22: power amplifier circuit



It contains a common-emitter amplifier that provides a small gain to the extracted carrier (the LPF's output). Then, a push-pull (Class AB) amplifier is used in to order to deliver greater currents to the antenna (represented by the resistance R2). The transistors are biased using two current-mirror subcircuits that provide a reliable DC bias. Also, by using the push-pull amplifier, the overall efficiency is increased, since only one transistor is active each time.

4 RESULTS AND REMARKS

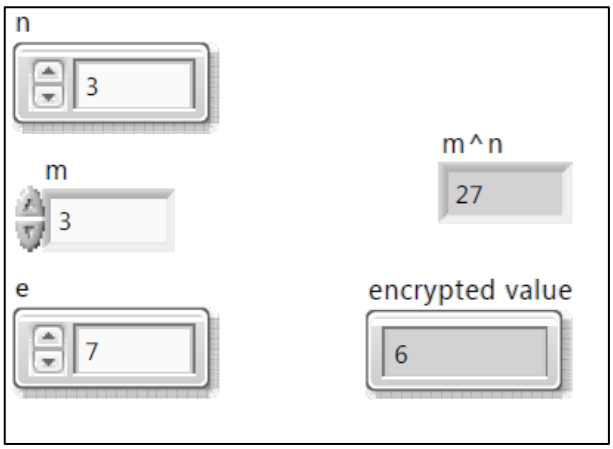
The transmitter system, shown in the Figure 15, was simulated and assembled into a laboratory proto-board by parts. The simulation was done on the NI Multisim 13.0, LabVIEW 2014 and ADS 2014. The results for each module or circuit are presented in the next subsections.

4.1 Encryption and Channel Coding

The LabVIEW schematic was tested against a set of public keys (i.e. values n and e). For all values, the encryption module provided the expected result given by the formula presented in Equation 32. Figure 23 shows an example for $n = 3$ and $e = 7$.

$$c = m^n mod(e) \tag{32}$$

Figure 23: RSA encryption on real-time, example



The encrypted values were then converted to a number in which the binary equivalent would be the encrypted value plus a parity bit justified at the right side. The table 1 presents the results obtained for a few tests. For all cases, the value of the message (m) is 33.

Table 1: encrypted values and parity bits

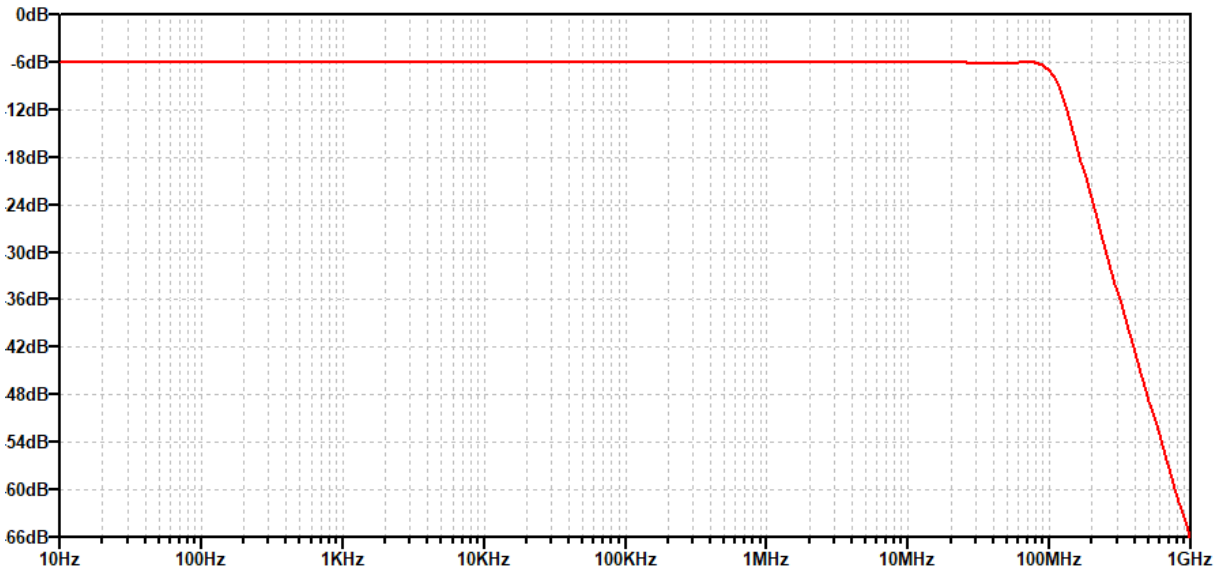
n	e	Encrypted value (EV)	EV (binary)	EV + parity bit	EV + parity bit (binary)
2	2	1	0001	3	00011
2	10	9	1001	18	10010
6	3	0	0000	0	00000
6	4	1	0001	3	00011
10	5	4	0100	9	01001
10	7	2	0010	5	00101
62	61	0	0000	0	00000

4.2 Filters

Simulation results for the carrier extraction circuit

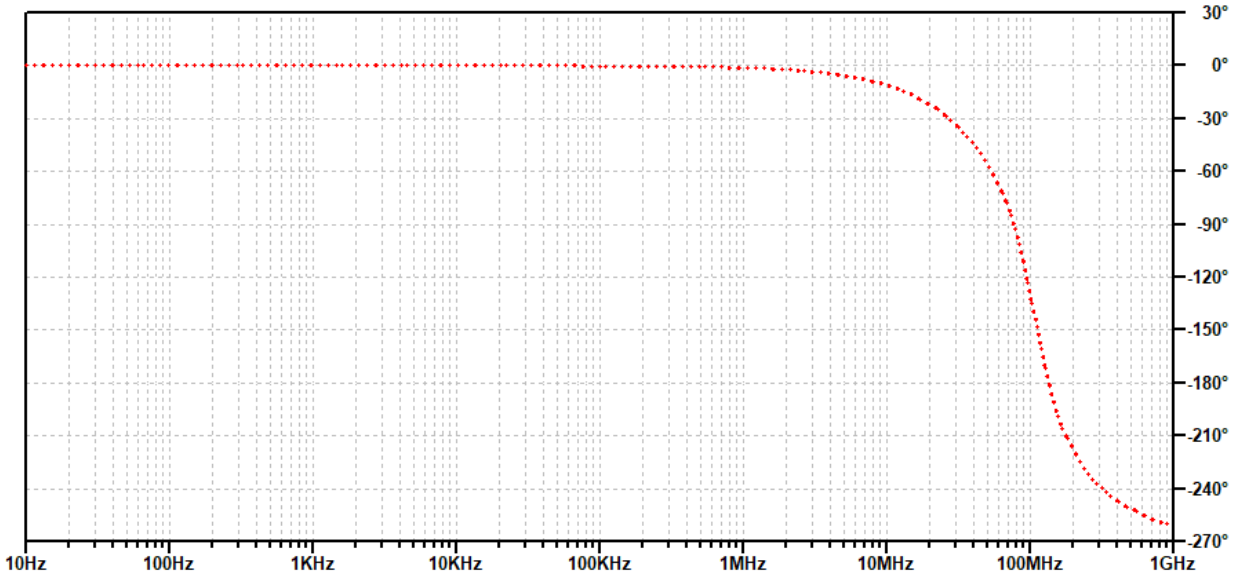
The circuit for the analogue carrier extraction, i.e. the low-pass filter (shown in the Figure 19) was simulated regarding to its S-parameters. Figures 24 and 25 show the frequency response for the simulation of this circuit, whose cut-off frequency was set around 116MHz in order to attenuate in the signal all harmonics but the first.

Figure 24: low-pass filter gain



The circuit is a Butterworth filter of order 3. So, as expected, after the cut-off frequency the gain decreases at a ratio of about -60dB/dec. For frequencies bellow 100MHz, the filter has a rather flat frequency response with little attenuation for incoming signals at these frequencies. Also, this filter has the advantage of not having (or having very little) pass band ripple -- when compared to a Chebyshev filter of the same order, for instance.

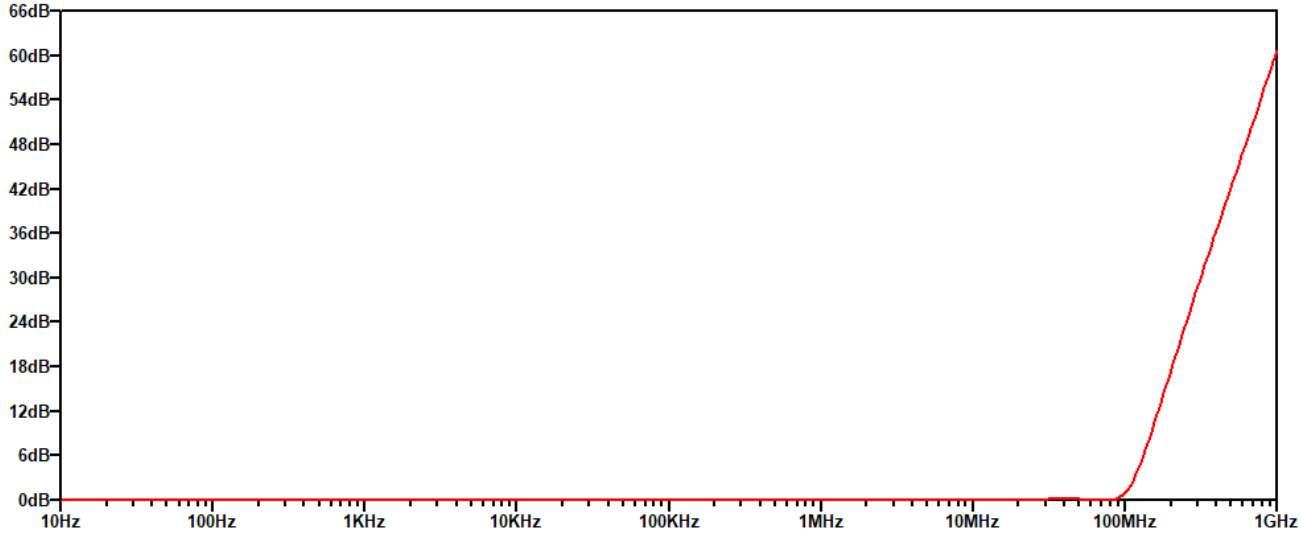
Figure 25: low-pass filter phase shift



There is a phase shift for the recovered carrier of about 60º. However since the sole purpose of the filter is to extract the first harmonic of the signal (at 88MHz), this phase shift has not impact or influence for the rest of the system.

Insertion Loss of the carrier extraction circuit

Figure 26: insertion loss for the low-pass filter



As expected, the inserted loss for the harmonics above the cut-off frequency grows rapidly – which guarantees that little of the high harmonics from the original square wave will be presented in the output signal.

Band Pass Filters

Every RF amplifier in the system is followed by a band pass filter in order to reduce harmonic contribution, noise and interference. The band-pass filter designed, shown in the Figure 20, was simulated regarding to its S-parameters. Figures 27 and 28 show the frequency response for the simulation of this circuit. The filter was designed with a bandwidth of approximately 46MHz and with centre frequency of 88MHz.

Figure 267: band-pass filter gain

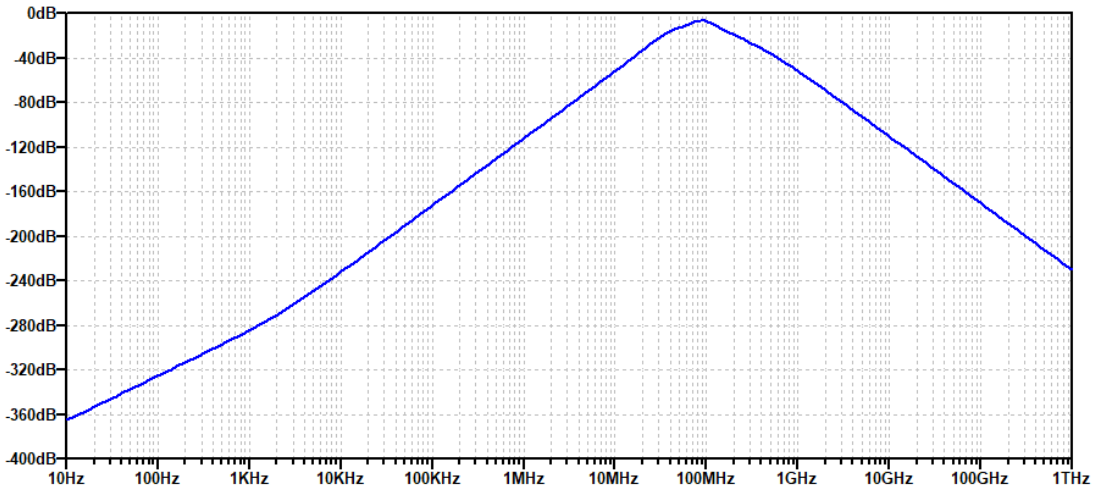
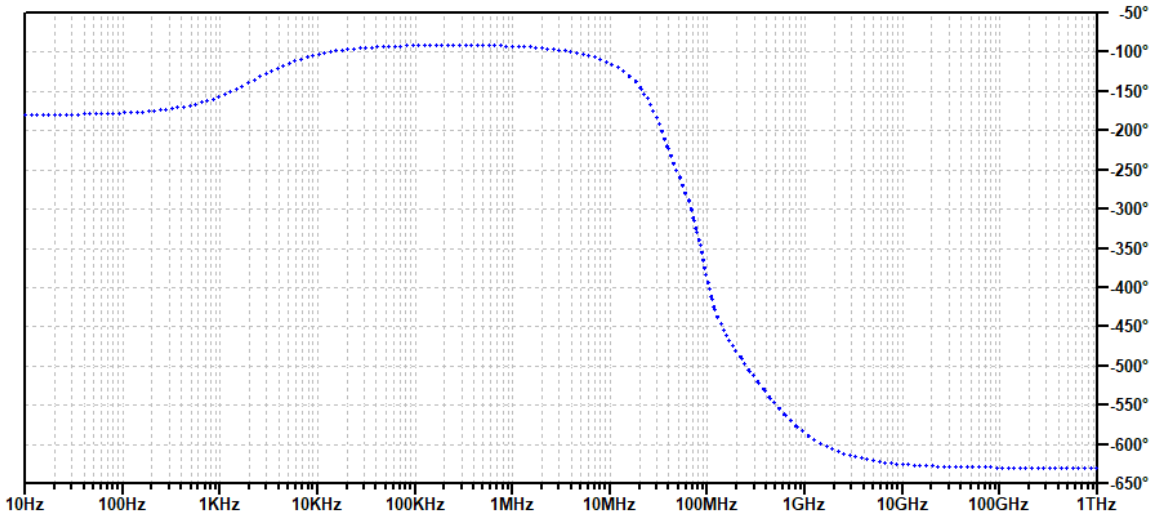
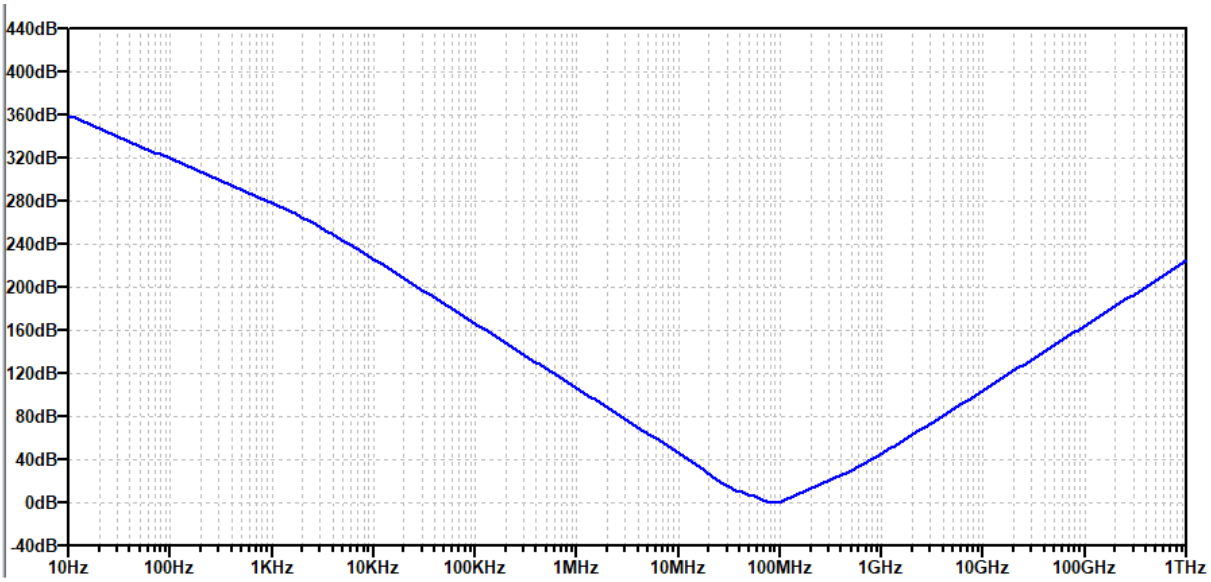


Figure 278: band-pass phase shift



Insertion Loss

Figure 29: insertion loss for the band-pass filter



4.3 Modulation

The BPSK modulator shown in the Figure 21 was simulated and implemented into a proto-board. The time-based results for simulation and proto-board circuit for this modulator is shown in the Figures 30 and 31, respectively .

Figure 30: simulation of the BPSK modulator; the output is shown in green.

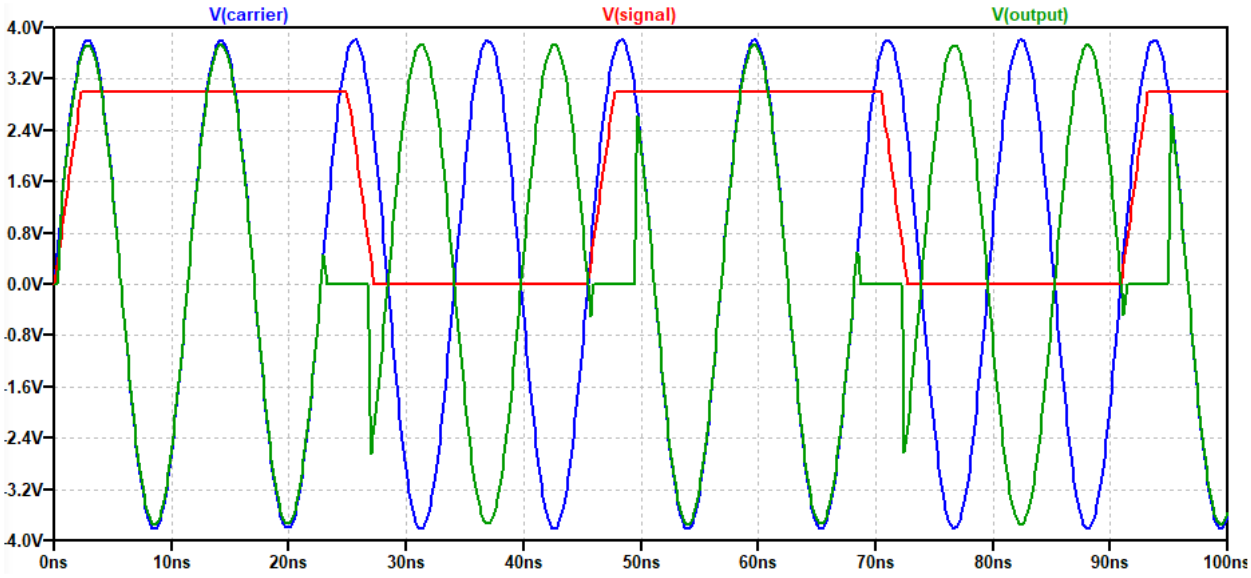
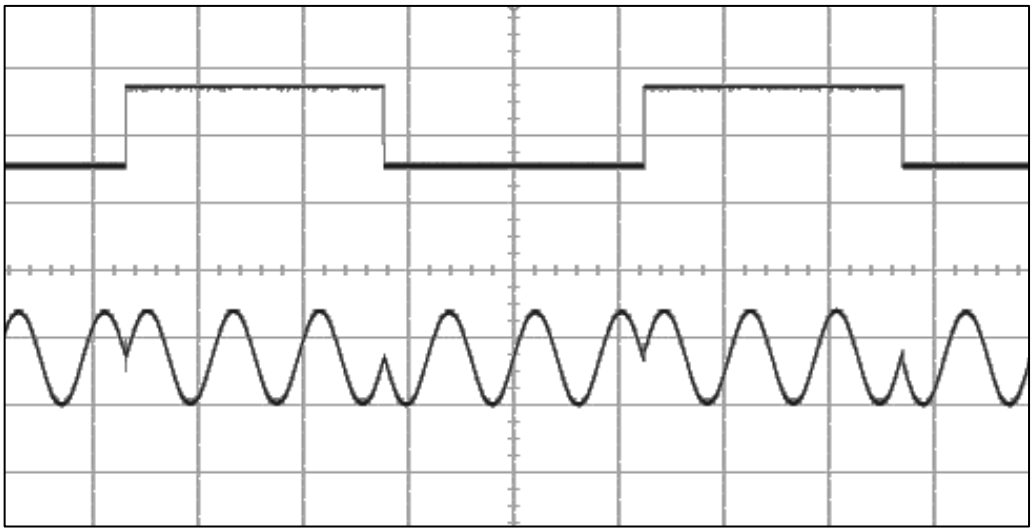


Figure 31: colored picture of the BPSK modulator's output and modulating signal (modulating signal amplitude: 3V, output signal amplitude: 3.8 V; time per division: 10ns)



Spectrum results for the BPSK Modulator

The simulated circuit was also analised regarding to its response on the frequency domain using a carrier wave of 88MHz provided by an ideal analogue voltage source with 50Ω series resistance and a modulating signal composed of a 20MHz square wave. The obtained carrier wave spectrum (in log-scale) and square wave spectrum (in linear sale) is shown in Figures 32 and 33, respectively.

Figure 32: carrier wave spectrum in log-scale

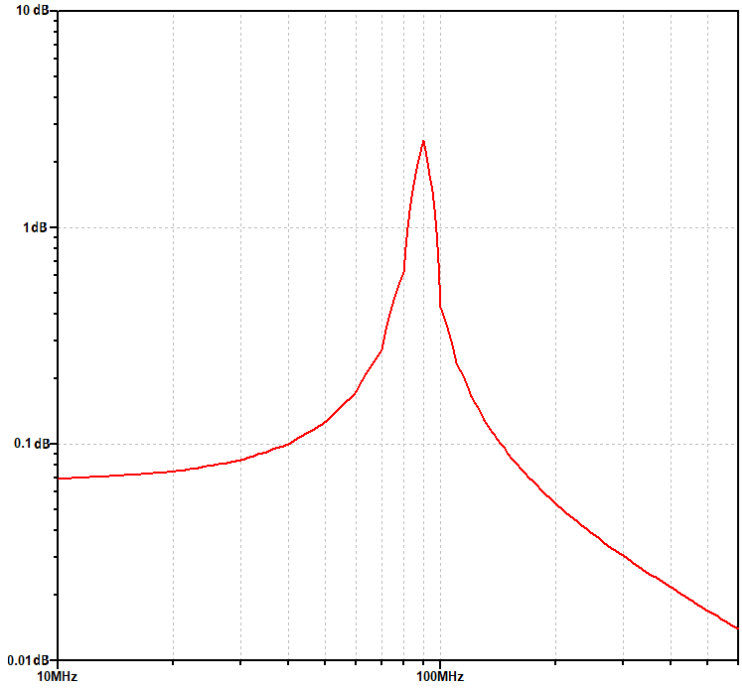
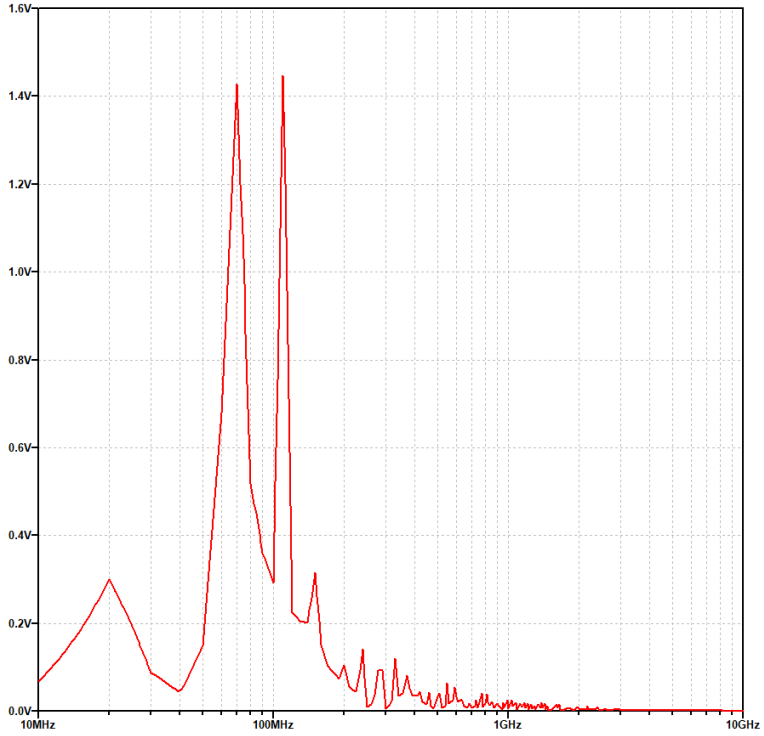


Figure 33: square signal wave spectrum in linear-scale

The output spectrum for the BPSK modulator for the input signals described above is shown in the Figure 34.

Figure 34: modulated signal spectrum in linear-scale



The peaks are around 68MHz and 108MHz, which correspond to the two main Fourier components of the mixed signal, as expected according to the Equations 26 and 27.

4.4 Power Amplification

The power amplifier designed, shown in Figure 22, was simulated and implemented into proto-board. The input-output response for them is shown in the Figure 35 and 36, respectively.

Figure 35: power amplifier simulation

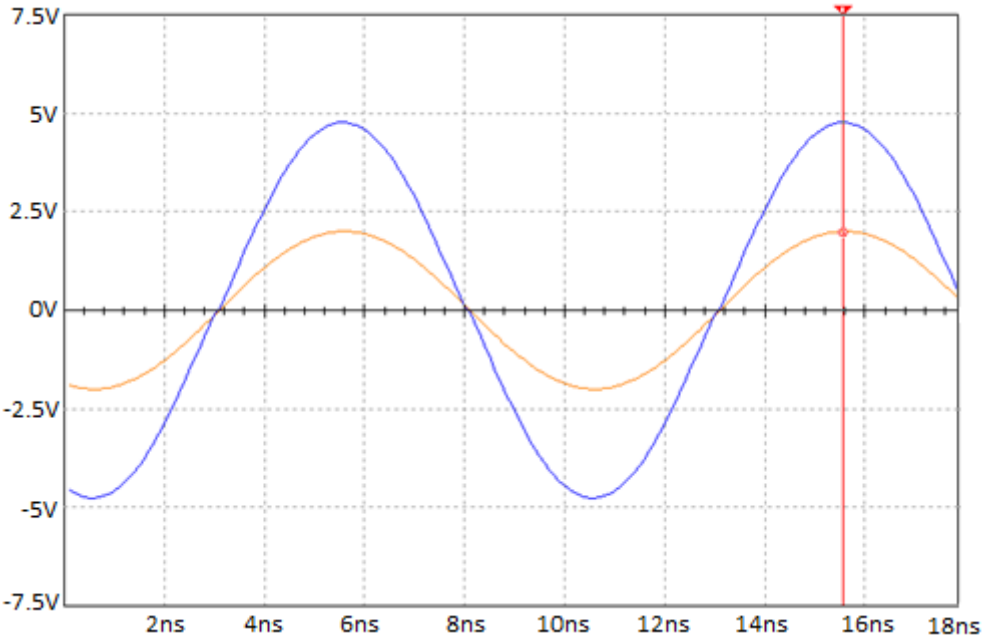
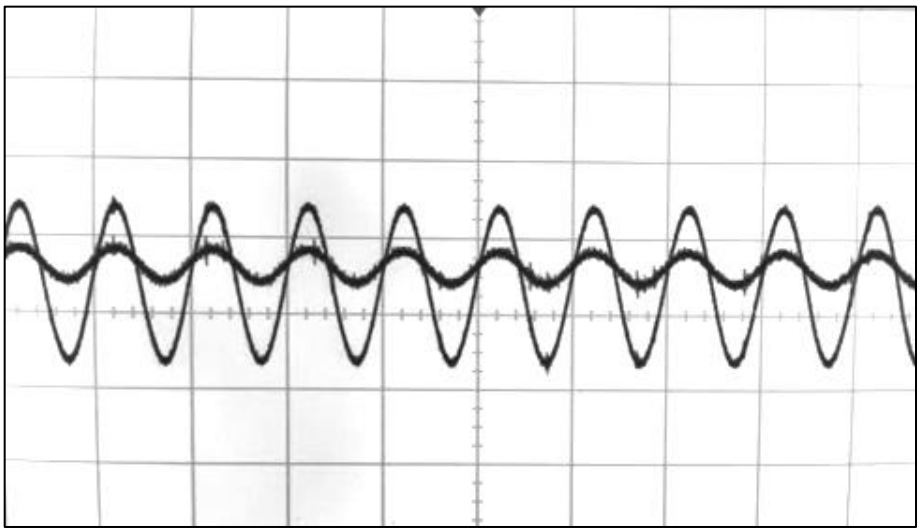


Figure 36: colored picture for the measurements of the power amplifier response on proto-board (input amplitude: 3.8 V; output amplitude: 5V; time per division: 10ns)



Spectrum results for the power amplifier

The frequency response for the power amplifier is shown in the Figures 37, 38 and 39, corresponding to the output voltage gain, a zoom-in view of the output voltage gain around the frequencies of the modulated signal and phase shift response, respectively.

Figure 37: power amplifier gain

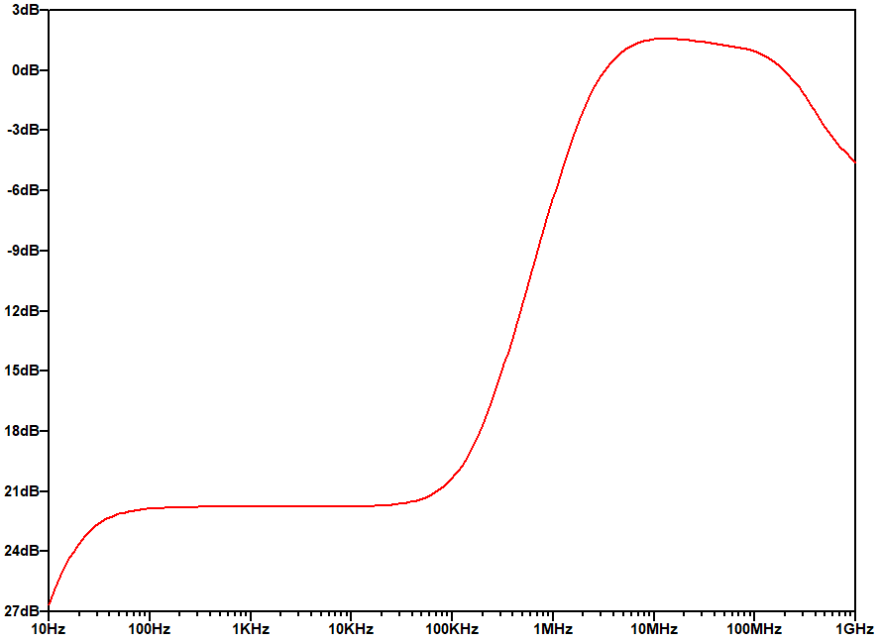


Figure 38: power amplifier gain around the modulated signal frequencies

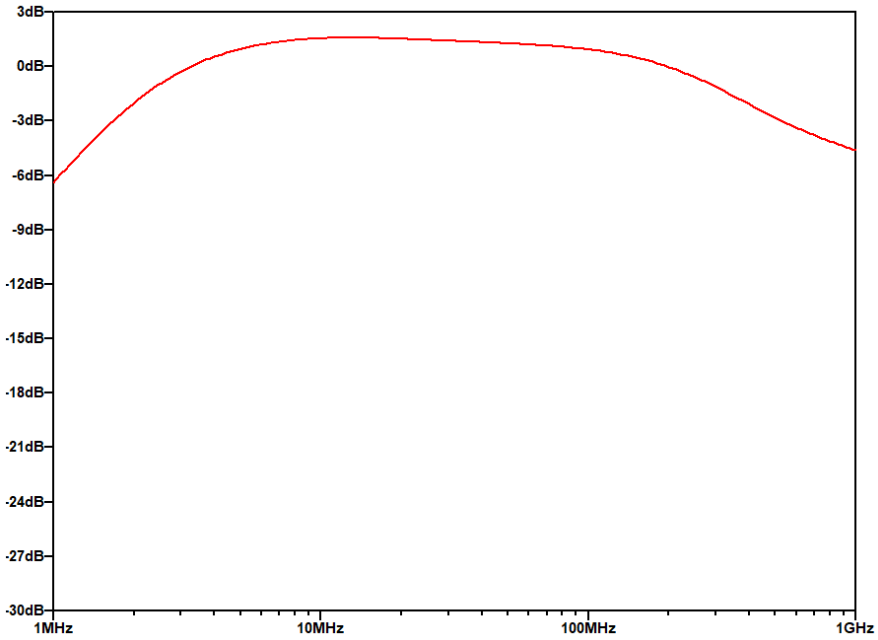
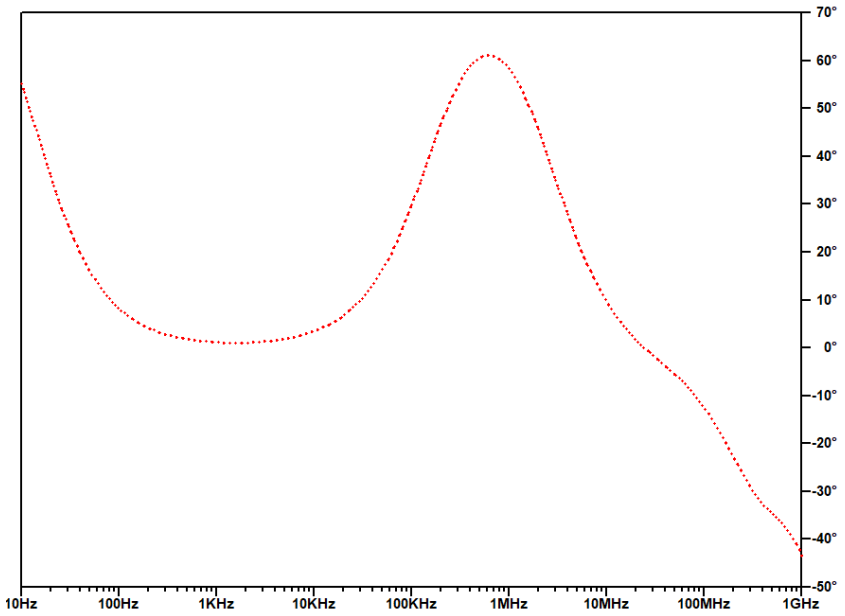
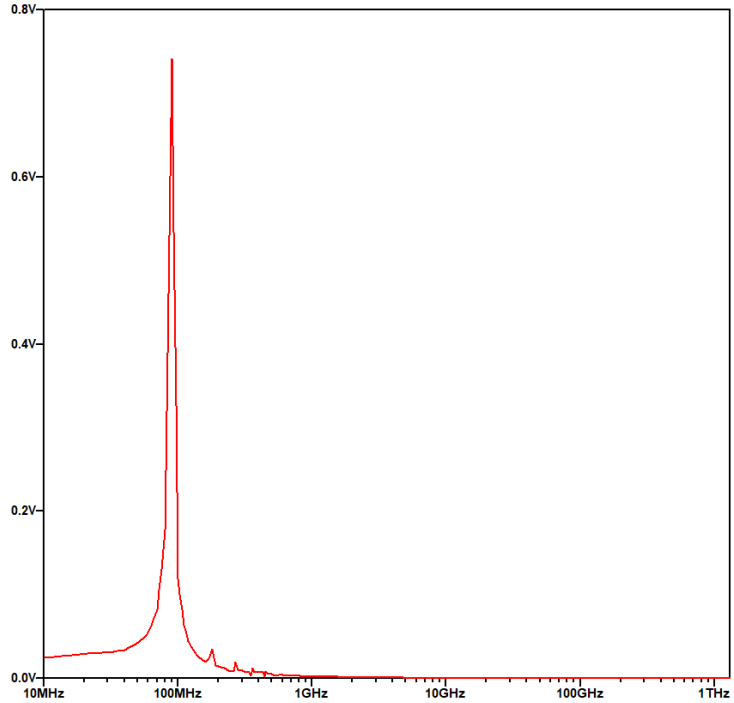


Figure 39: power amplifier phase shift



The amplifier was designed to provide a high current gain to the antenna while keeping unitary voltage gain. The results shown that the voltage gain is more or less constant and unitary from around 8MHz until 115MHz. This bandwidth covers well the output spectrum for the modulated signal. However, the amplifier also works as an interesting band-pass filter for frequencies outside this bandwidth. Figure 40 presents the spectrum for the amplification of the modulated signal after the amplifier was connected to the rest of the system

Figure 40: amplified 88MHz signal spectrum



Output signal harmonics and THD

As an active circuit, the amplifier also introduces harmonics to the output signal. The Figure 41 shows the simulation results for the total harmonic distortion (THD) analysis for the circuit.

Figure 41: simulation results for the output signal harmonics

Harmonic Number	Frequency [Hz]	Fourier Component	Normalized Component	Phase [degree]	Normalized Phase [deg]
1	8.800e+07	1.112e+00	1.000e+00	-10.03°	0.00°
2	1.760e+08	4.916e-02	4.419e-02	110.93°	120.96°
3	2.640e+08	2.732e-02	2.456e-02	126.06°	136.10°
4	3.520e+08	2.146e-02	1.929e-02	149.39°	159.42°
5	4.400e+08	1.648e-02	1.481e-02	171.52°	181.56°
6	5.280e+08	1.263e-02	1.136e-02	-164.39°	-154.36°
7	6.160e+08	9.688e-03	8.710e-03	-139.35°	-129.32°
8	7.040e+08	7.360e-03	6.617e-03	-113.31°	-103.27°
9	7.920e+08	5.503e-03	4.947e-03	-85.82°	-75.78°
10	8.800e+08	4.037e-03	3.629e-03	-56.12°	-46.09°

Total Harmonic Distortion: 5.860390%(5.878801%)

Considering that high order harmonics affect considerably the transmitter performance in regards to bit error rate, the results suggest that this power should be further improved in order to accomplish a lower THD and better power efficiency performance.

5 CONCLUSIONS

This project aim was to design a complete telecommunication system based on myRIO and bespoken circuits. Although the task was slightly daunting, the results are as expected from the theoretical point of view. A great deal of concepts in communication system was implemented in the project, proving the great capabilities of simple and accessible platforms like the myRIO together with tailored electronic circuits - filters, mixers and amplifiers were integrated to produce a compact yet robust proto-board solution for the BPSK transmitter and receiver. So that it was possible to create a reliable, encrypted and fast digital VHF point-to-point link. The project can be continued or improved by implement other complex modulation schemes, such as QPSK, as well as line coding.

Personally, I have learned a great deal with the task – especially in the difficult external circumstances that it was accomplished. Thanks for all those who supported it somehow.

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